Analog content-addressable memories with 2D floating-gate memory transistor

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In the era of Big Data, the data transfer bottleneck in data-intensive applications demands in-memory computing hardware, for efficient processes on edge devices. Content addressable memories (CAM) are in-memory computing with commercial success because they offer extremely high throughput but at the expense of high energy consumption. Therefore, applications are limited to highly specialized scenarios, such as network routing. Analog CAM[1-2] has been proposed recently to further increase memory density and reduce energy consumption. Still, silicon-based transistors have bottlenecked the performance and prevented the three-dimension stack-ability.

Here, we propose and build analog CAM based on two-dimensional (2D) floating gate field-effect transistors (FGFET) to tackle bottlenecks imposed by silicon transistors. 2D transition metal dichalcogenides (TMDs), *i.e.*, MoS_2, based FGFETs offer atomic-scale thickness channel, high current ON/OFF ratio, ideal subthreshold characteristics even at nanoscale gate length, relatively high mobility, negligible drain capacitance, large memory window, and appealing 3D stackability[3-5]. Therefore, it would be an ideal candidate for building analog CAM.

Our proposed 2D FGFET analog CAM cell is composed of two MoS_2 FGFETs connected in parallel (Fig.3a). Fig. 1&2 show the fabrication process of a 2×8 devices array. Benefiting from the 2D property of monolayer MoS_2 continuous film and high-κ dielectric (HfO_2), the device shows a small program voltage, a steep subthreshold slope, and a large memory window(~3V) with a large memory ON/Off ratio (10^8) (Fig.3b). The threshold voltage of each transistor, representing the lower and higher searching bound of analog CAM respectively, can be continuously tuned by program pulses to the control gate. Fig. 3c demonstrates that the searching higher bound can be tuned experimentally in our physical analog CAM. Fig. 3d shows the simulated operation with our custom experimentally validated model. We expect large-scale 2D FGFET-based analog CAM to be a promising build block for a near-sensor explainable tree-based machine learning accelerator. Our findings highlight the potential of atomically thin semiconductors for developing next-generation high-speed and low-power edge devices.

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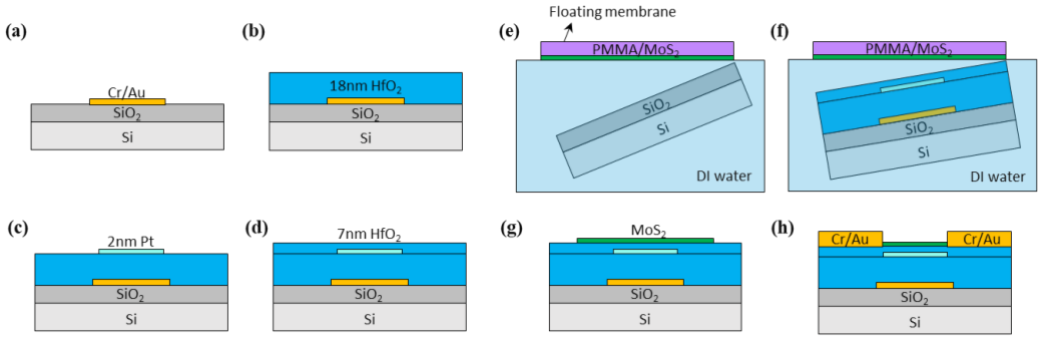

Figure 1: The schematic of fabrication processes of MoS_2 floating-gate memory transistors. (a) Prepare bottom gate with photolithography, depositing 5/40nm Cr/Au, and liftoff process. (b) Cover the bottom gate with 18nm HfO_2 by ALD. (c) Prepare floating gate with photolithography, depositing 2nm Pt, and liftoff process. (d) Cover the floating gate with 7nm HfO_2 by ALD. (e) Transfer monolayer MoS_2 continuous film with PMMA in DI water. (f) Pick up floating PMMA/MoS_2 membrane by the prepared substrate. (g) Dissolve PMMA in acetone and pattern MoS_2 film with RIE. (h) Prepare contact electrodes with photolithography, depositing 5/40nm Cr/Au, and the liftoff process. In all the photolithography processes, a double-layer photoresist (LOR/AZ5214E) was used for easy lift-off.

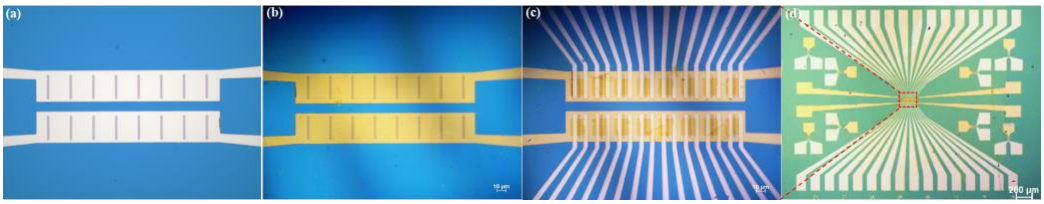

Figure 2: The Optical microscope images of MoS_2 floating-gate memory transistors array. (a) The prepared substrate with 18 nm HfO_2 as the blocking oxide layer, 2 nm Pt as the floating gate, and 7 nm HfO_2 as the tunnelling oxide layer. (b) Monolayer MoS_2 Continuous film was transferred to the prepared substrate. (c) As-fabricated devices array. The scale bars, 10μm. (d) The overall view of the final devices array. The scale bar is 200μm.

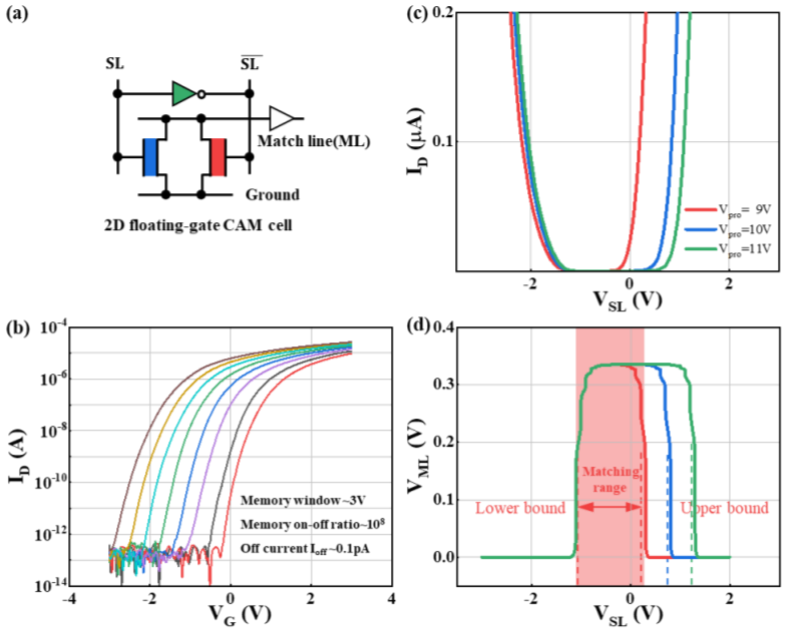

Figure 3: The electrical performance of the analog CAM based on two MoS_2 FGFETs. (a) Schematic of our proposed 2D floating-gate analog CAM circuit, composed of two MoS_2 FGFET, a clocked inverter for the search line (SL), and a sense amplifier (SA) for the match line (ML). Voltage amplitude on the SL provides search input and the matching result is sensed on the ML. (b) Programmed I_D-V_G transfer characteristic curves of the MoS_2 FGFET with different program voltages (6V~10V). (c-d) The test and simulation results of the 2D floating-gate CAM cell for matching with different voltage ranges, i.e., a fixed lower bound and three different upper bounds. These bounds were determined by the programmed V_{th} of the two floating-gate memory transistors. The search input voltage was applied on the search line and control gate, and the voltage on the ML will keep if the input voltage value is within the matching range.