## Fabrication and Characterization of MoS<sub>2</sub> Memristive Devices with Short and Long-Term Memory Behaviors

Seungjun Ki, Mingze Chen, and Xiaogan Liang\*

Mechanical Engineering Department, University of Michigan, Ann Arbor, MI 48109

Transition-metal dichalcogenides (TMDs) have attracted significant interest as promising candidates for future electronic and optoelectronic device applications, with highly anisotropic electrical transport characteristics due to their layered crystal structures. More recently, memristor-like response characteristics have been also observed in the nano- and microelectronic devices made from 2D-layered TMDCs, such as MoS<sub>2</sub> and WSe<sub>2</sub> [1-3]. Such emerging 2D-material-based memristive devices (*e.g.*, memtransistors and memristors) could be deployed for constructing novel hardware-based neural network systems with a significantly improved level of interconnectivity and potentially enabling emulation of biological neuron functions [4-5]. In addition,  $MoS_2$  memristors have been also investigated for emulating synaptic responses since the relevant mechanisms such as charge trapping and migration of ionic vacancies are greatly prominent in the layered structure of such TMDs materials [6-7].

One of the subsequent research efforts seeks to emulate the memory processes in the human brain, which have been modeled involving two types of synaptic plasticity: short-term plasticity (STP) and long-term potentiation (LTP) [8-9]. STP is the temporal synaptic response of a synapse to activity or action patterns through synaptic connections (or networks). LTP is a permanent change (or a change with long-term retention) of the synaptic response weight induced by repeated stimulations with relatively short intervals. Recent studies demonstrated MoS<sub>2</sub>-based memristive and field-effect devices exhibiting both STP-like and LTP-like transport behaviors [6-7].

In this work, we present a study on the memristive devices made from mechanically exfoliated multilayer MoS<sub>2</sub> films. We fabricated two-terminal memristors with multi-layer MoS<sub>2</sub> channels and investigated pulse-programmed short-term and long-term synaptic responses (Figure 1a). MoS<sub>2</sub> memristors exhibit both STP and LTP synaptic response characteristics when subjected to time-sequential voltage pulses. Specifically, we applied a queue of voltage pulses with different pre-set amplitudes, polarities, periods, duty cycles, and numbers of applied pulses (Figure 1b). During such a pulse-programmed potentiation process, the electrical conductance of the  $MoS_2$ memristor increases with the lapsed time or the number of applied pulses (Figure 1c). After the potentiation process, *i.e.*, application of all programming pulses for each test run, the conductance of the MoS<sub>2</sub> memristor starts to decrease during the relaxation process. After the measurement, we utilized the paired-pulse facilitation (PPF) function for fitting the experimentally measured relaxation curves of MoS<sub>2</sub> memristors to quantitatively evaluate the relative dominance of STP and LTP effects. The fitting results indicate that the magnitudes of both STP and LTP terms measured from a memristor increase with increasing pulse frequency, pulse amplitude, pulse duty cycle, and a total number of applied pulses (Figure 1d). We further investigated the correlation between other pulse parameters (i.e., polarity, period, duty cycle, and the number of applied pulses) and two types of potentiation effects effects.

This work provides a useful guideline for activating STP and LTP effects in emerging memristive devices based on 2D layered semiconductors, which could be deployed for making synaptic nodes in hardware-based artificial neural networks or neuromorphic sensory devices capable of sensing spatiotemporal events.



Figure. 1 (a) Illustration of a MoS<sub>2</sub> memristor; (b) illustration of the voltage pulse with denoted parameters; (c) pulse-programmed characteristic curves measured at different pulse amplitudes (or voltages) of 1V, 3V, 5V, 7V, 9V and fixed pulse width ( $\Delta t_{pulse} = 1ms$ ), pulse duty cycle of (D = 50%), and pulse period of (( $\Delta t_{period} = 2ms$ ); (d)  $C_1$  and  $C_2$  coefficients extracted from the PPF function fitting (red lines shown in (c)) plotted as the function of pulse voltage amplitudes;

## REFERENCES

[1] X. J. Zhu, D. Li, X. G. Liang, and W. D. Lu, "Ionic modulation and ionic coupling effects in MoS2 devices for neuromorphic computing," *Nature Materials*, vol. 18, pp. 141-+, Feb 2019.

[2] V. K. Sangwan, H. S. Lee, H. Bergeron, I. Balla, M. E. Beck, K. S. Chen, *et al.*, "Multi-Terminal Memtransistors from Polycrystalline Monolayer MoS<sub>2</sub>," *Nature*, vol. xx, p. xx, 2018.

[3] V. K. Sangwan, D. Jariwala, I. S. Kim, K. S. Chen, T. J. Marks, L. J. Lauhon, *et al.*, "Gate-tunable memristive phenomena mediated by grain boundaries in single-layer MoS2," *Nature Nanotechnology*, vol. 10, pp. 403-406, May 2015.

[4] D. Li, B. Ryu, J. Yoon, Z. R. Li, and X. G. Liang, "Improvement of analogue switching characteristics of MoS2 memristors through plasma treatment," *Journal of Physics D-Applied Physics*, vol. 53, Mar 25 2020.

[5] D. Li, B. Wu, X. J. Zhu, J. T. Wang, B. Ryu, W. D. Lu, *et al.*, "MoS2 Memristors Exhibiting Variable Switching Characteristics toward Biorealistic Synaptic Emulation," *ACS Nano*, vol. 12, pp. 9240-9252, Sep 2018.

[6] P. F. Cheng, K. Sun, and Y. H. Hu, "Memristive Behavior and Ideal Memristor of 1T Phase MoS2 Nanosheets," Nano Letters, vol. 16, pp. 572-576, Jan 2016.

[7] M. Chen, H. Nam, S. Wi, G. Priessnitz, I. M. Gunawan, and X. Liang, "Multibit Data Storage States Formed in Plasma-Treated MoS2 Transistors," ACS Nano, vol. 8, pp. 4023-4032, Apr 22 2014.

[8] D. G. Zakharov and A. S. Kuznetsov, "On the dynamical mechanisms of influence of synaptic currents on the neuron model with response differentiation," *Jetp Letters*, vol. 102, pp. 184-188, Aug 2015.

[9] M. A. Gainey, V. Tatavarty, M. Nahmani, H. Lin, and G. G. Turrigiano, "Activity-dependent synaptic GRIP1 accumulation drives synaptic scaling up in response to action potential blockade," *Proceedings of the National Academy of Sciences of the United States of America*, vol. 112, pp. E3590-E3599, Jul 7 2015.