Direct integration of atomic precision devices with CMOS

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Modern semiconductor manufacturing has shrunk top-down processing to the near-atomic scale, where it has encountered new, and often fundamental limitations. Techniques that enable control over the atomic scale may identify new opportunities, but the inability to leverage past investments in CMOS can make identifying their potential impact difficult. Atomic Precision Advanced Manufacturing (APAM) enables the creation of atomically abrupt doping profiles, down to single-dopant and sub-nm precision using a scanned probe, or high throughput using light. Here, we describe a series of innovations that enables direct integration of APAM into middle-of-line CMOS manufacturing. We conclude by identifying several opportunities in microelectronics for APAM processing.

APAM relies on area-selective chemistry, where dopant precursors adsorb on depassivated regions of a hydrogen-terminated silicon surface, to define doped regions at the surface before preserving them under a layer of low-temperature silicon epitaxy. This technique has mostly been used to make cryogenic devices, such as qubits[1], but has recently been shown to produce devices robust to accelerated lifetime testing well above room temperatures[2]. The primary technical challenge to CMOS integration lies in two thermal issues: the high temperature (1000° C) needed to produce a required atomically ordered surface, which limits processing that precedes APAM; and the low temperature (500° C) at which the incorporated dopants start to diffuse, which limits processing that follows APAM. We have identified an insertion point between high temperature front-end-of-line processing, and low temperature back-end-of-line processing, which can accommodate a ~650° C process (Fig. 1). At this thermal envelope, we have developed a sputter and anneal process which produces an atomically ordered surface (Fig. 2). Working circuits that incorporate both APAM and CMOS devices provide a proof-of-concept (Fig. 3)[3].

We conclude by providing a glimpse into three potential applications: CMOS transistor contacts for reduced resistance, single electron transistors for enhanced sensors, and vertical tunnel field effect transistors for low power digital circuits. *SNL is managed and operated by NTESS under DOE NNSA contract DE-NA0003525.*

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[1] Y. He, *et al.*, *Nature* **571**, 371-375 (2019). X. Wang, *et al.*, *Comm. Phys.* **3**, 82 (2020).

[2] C. Halsey, *et al.*, *IEEE Trans. Dev. Mater. Rel.* **22**, 169-174 (2022).

[3] D. Ward, *et al.*, US Patent Application 17/360,284.

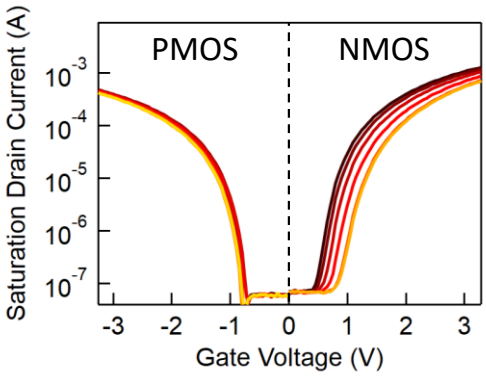

Figure 1: Annealed transistor I_D-V_{GS}. PMOS transistor I_D-V_{GS} were unchanged after annealing at temperatures ranging from 600 – 850° C (black to yellow), while NMOS transistor I_D-V_{GS} changed significantly above 650° C.

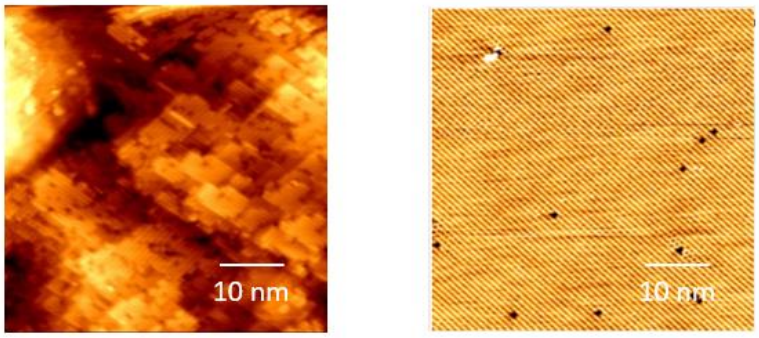

Figure 2: Atomic order of sputter/anneal process. Images of the silicon surface after an Ar ion sputter followed by a 650° C anneal (left) and an 800° C anneal (right). The former is ordered but stepped, while the latter is pristine.

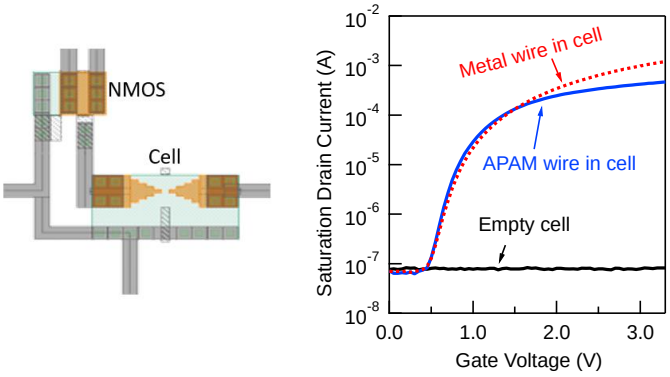

Figure 3: CMOS + APAM circuit. (Left) Schematic diagram of NMOS transistor gate driven by different passives fabricated in the cell. (Right) The I-V curve of the NMOS transistor with a metal wire driving the gate (red), with an APAM wire driving the gate (blue), or with the cell left empty (black).