Improving AlOx based Single Electron Transistors for Quantum Charge Sensing

<u>R. Li^{1, 2}</u>, P. Namboodiri¹, Zachary Barcikowski^{1, 2}, Y. Hong^{1, 2}, J. M. Pomeroy¹ ¹National Institute of Standards and Technology, Gaithersburg, MD 20899 ²University of Maryland, College Park, MD 20742 rnl10@nist.gov

The resistance of aluminum oxide (AlOx) thin films is explored by varying the plasma oxidation duration, which can reduce the RC (resistance*capacitance) time constant and improve the bandwidth of charge sensors. In our prior work, similar AlOx based single electron transistors (SETs) were shown to be sufficiently stable for incorporation as qubit charge sensors, but still lack sufficient bandwidth. Our approach has stabilized the devices, motivating our efforts to increase the bandwidth. The precise control of the oxidation chemistry is accomplished using a custom, UHV oxidation chamber linked *in situ* to a deposition chamber to produce the AlOx thin film without any exposure to atmosphere. Typically, the stabilized devices have a high resistance at $\approx 10^8 \Omega$, limiting the bandwidth at a few kHz. Our current goal is to produce AlOx thin films that allows the SETs we manufacture to work at >1MHz.

To develop the oxide recipes, resistance and capacitance values for large area ($\approx 3000 \ \mu m^2$) tunnel junctions made with different oxidation times through *in situ* mechanical shadow masks are made, rather than making complete SET devices. The large area tunnel junctions are fabricated by a 3-step process with electronbeam metal deposition and plasma oxidation applied in the middle to produce the oxide for tunnel junction. The large area tunnel junction pattern is defined with metal shadow masks set in front of the blank wafers; a completed device wafer is shown Fig. 1. After fabrication, the resistance of devices with similar areas are found to systematically increase with oxidation time as expect, preliminary data is shown in Fig. 2.



Fig. 1 – An oxidized, 75 mm Si handle wafer with an array of tunnel junction dies fabricated on top in various patterns.



Fig. 2 –Tunnel junction resistances for device A1A (first of four tunnel junctions on the top left die of the wafer shown on Fig. 1) when made using 5 s, 6 s, 7 s and 8 s of oxidation time. The error bars represent 2 sigma deviation from the mean. No type B uncertainties are considered