Improving Current On/Off Ratio of Oxygen-Doped WSe_2 transistors by Selective Scanning Probe Lithography

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WSe_2 is a prototypical p-type 2D semiconductor for nano-electronics, but its transistor performance remains contact-limited. Fermi level pinning at the metal-semiconductor interface causes large Schottky barriers.[1] One potential solution is to degenerately dope WSe_2 in the contact region to reduce the Schottky barrier width to facilitate tunneling. Oxidizing the topmost layer of WSe_2 results in stable hole doping without damaging underlying WSe_2 layers, achieving one of the lowest contact resistances in WSe_2.[2] However, degenerately doped WSe_2 channel cannot be turned off for use as transistors. Here we use a scanning probe to selectively remove WO_x on WSe_2, which significantly improves the current on/off ratio of oxygen-doped WSe_2 transistors while preserving their high on-current.

Figure 1a shows the schematic of device fabrication. A gentle remote O_2 plasma process oxidizes the topmost layer of Pd/Au contacted tri-layer WSe_2 field-effect transistor (FET) on SiO_2/Si. Next, a diamond-coated atomic force microscope (AFM) tip[3] selectively scratches off WO_x on WSe_2 in contact mode.

Figures 1b and 1c show the AFM image of an example FET and its transfer curves as measured at each stage of fabrication. The FET had an on-current of 2.2 μA/μm and an on/off ratio of 4×10^4 as fabricated, an on-current of 46 μA/μm and an on/off ratio of 16 after remote O_2 plasma, and an on-current of 36 μA/μm and an on/off ratio of 3×10^5 after SPL. Selective removal of WO_x improved the current on/off ratio by 2×10^4 while the on-current decreased slightly by 22%.

Figure 2 benchmarks the performance of oxidized few-layer WSe_2 FETs in this work with the state-of-the-art p-type transition metal dichalcogenide transistors.

This works shows the potential of selectively oxidized few-layer WSe_2 to fabricate high-performance short channel transistors that meet the demand for next-generation electronics. The same selective SPL strategy can also be applied to other molecular dopants in fabricating short channel 2D transistors.

[1] Y. Xu, C. Cheng, S. Du, J. Yang, B. Yu, J. Luo, W. Yin, E. Li, S. Dong, P. Ye, and X. Duan, ACS Nano **10**, (2016).

[2] A. Borah, A. Nipane, M.S. Choi, J. Hone, and J.T. Teherani, ACS Appl. Electron. Mater. **3**, 2941 (2021).

[3] P.C. Fletcher, J.R. Felts, Z. Dai, T.D. Jacobs, H. Zeng, W. Lee, P.E. Sheehan, J.A. Carlisle, R.W. Carpick, and W.P. King, ACS Nano **4**, 3338 (2010).

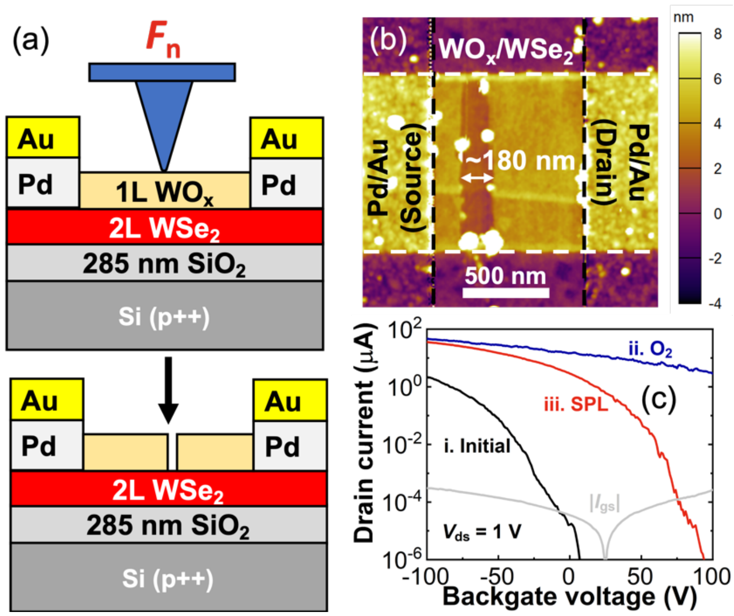

Figure 1: (a) Schematic of the use of an AFM tip to selectively remove monolayer (1L) WO_x on a bilayer (2L) WSe_2 FET. (b) AFM topography of an example FET shown in (a). (c) Transfer curves of the example FET as-fabricated (i. Initial), after remote O_2 plasma (ii. O_2), and after scanning probe lithography (iii. SPL). Gate leakage current $|I_{gs}|$ in stage iii is plotted in gray.

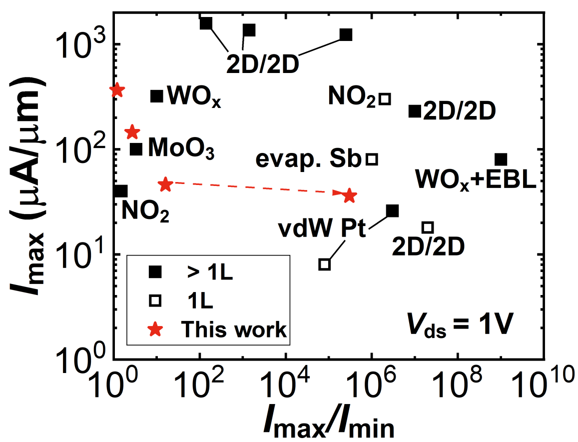

Figure 2: Benchmark plot of the state-of-the-art p-type transition metal dichalcogenide transistors with oxidized few-layer WSe_2 FETs in this work.