High aspect ratio arrays of silicon nanostructures with controllable tapered sidewall by non-ICP plasma DRIE

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High aspect ratio (HAR) nanostructures have gained significant interest due to their versatile applications in nano-optics. In the realization of HAR structures, a top-down dry etching process with a tailored sidewall profile, high selectivity, and controllable undercut is crucial. In addition, the surface roughness of the HAR structures plays an important role, impacting the light absorption and scattering within and at the surface of HAR nanostructures. Here we report on HAR lattices of plasma-etched silicon nanostructures with controllable tapered sidewalls using highly selective non-ICP plasma DRIE. Owing to their small surface roughness, these HAR nanostructures can be employed in direct nanoimprint lithography of HAR metasurface structures towards the realization of high-throughput lithography processes.

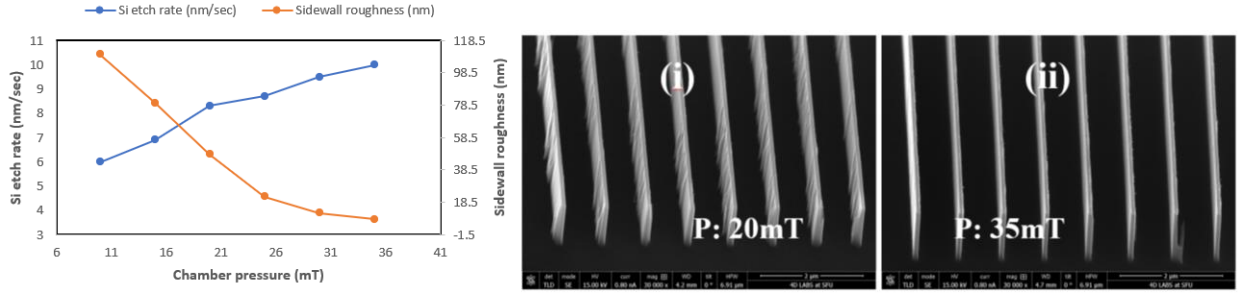
To realize the HAR nanostructures at the wafer scale, a positive resist was patterned using electron beam lithography followed by evaporating a thin layer of insulating aluminum oxide as the etch mask. Following an oxide lift-off process, the silicon layer was etched using a non-cycling pseudo-Bosch process employing a non-ICP plasma etcher. The non-switching etch process introduced here can simultaneously control the sidewall roughness and tune the sidewall profile from a largely positive (cone structure) to a largely negative (inverse cone structure) taper angle. The standard switching Bosch etch process results in rippled sidewalls in the etched silicon, making it unsuitable for some particular nano-optic applications.

Figure 1 (a) shows the silicon etch rate and the sidewall roughness of nanostructures as a function of the applied pressure in the chamber. Here, the effect of the process pressure was studied at a fixed gas flow of C4F8/SF6 and RF power, and at low temperatures. It is observed that increasing the chamber pressure leads to an increase in the number of accelerated ions, promoting the chemical etch and the overall etch rate. In this case, the fluorine ion acceleration is enhanced which leads to an increase of the ion bombardment at the perpendicular surfaces[i, ii]. However, a lower chamber pressure leads to a larger sheath space thickness under the main plasma region. As the accelerated ions must travel through a thicker sheath layer before reaching the sample, this results in a higher chance of collision with the gases in the plasma chamber, leading to a reduced physical etch rate. This also results in etching that is less directional. Sidewall roughness increases with reduced pressure due to the increase in plasma sheath thickness. Plasma sheath determines the plasma etchant energy and the strike angle of ions, which in turn determines the sidewall roughness of the etched silicon[iii]. This trend is confirmed by SEM imaging, as shown in figure 1b. We chose an optimal pressure range of 32 mTorr to 36 mTorr that minimizes sidewall roughness. In this pressure range, etch rate is also slow enough to avoid generating excessive local heat by ion bombardments. In doing so, we further minimize surface roughness, as local heat generation also leads to an increase in roughness.

Figure 2(a) shows the effect of C4F8 flow rate percentage on the etch rate of silicon and the sidewall angle in the non-switching etch recipe employed here. Unlike the etch rate, the taper angle increases as a function of C4F8 gas flow rate percentage in the range where the RF power and other parameters are kept unchanged except the chamber pressure. To explain the observed behavior, reviewing previous findings of the etch mechanism is helpful. It is shown that plasma etching of silicon with fluorinated chemistry is mainly due to free fluorine ions[iv]. By decreasing C4F8 gas flow rate percentage, the percentage of SF6 gas is increased. Since electron impact dissociation reactions involve SF6, increasing SF6 flow rate percentage leads to the increased fluorine ion concentration in the plasma mixture, which leads to higher silicon etch rates[v,vi]. At a higher C4F8 flow rate percentage, the number of passivation compounds increases and results in a reduction of the silicon etch rate in the horizontal direction which may lead to a positively tapered profile. Based on the same logic, sidewalls become negatively tapered at lower C4F8 flow rate percentages. As a result, the ratio of SF6 and C4F8 mixture is important to achieve a controlled etch rate and sidewall profile [vii,viii, ix]. However, decreasing the C4F8 flow rate also makes the surface rougher, so the chamber pressure needs to be varied in line with changing C4F8 gas flow to achieve an acceptably smooth surface. In figure 2 (b), SEM images demonstrate that increasing the C4F8 flow rate leads to an increase of the sidewall tapered angle from negatively tapered to positively tapered at a certain chamber pressure.

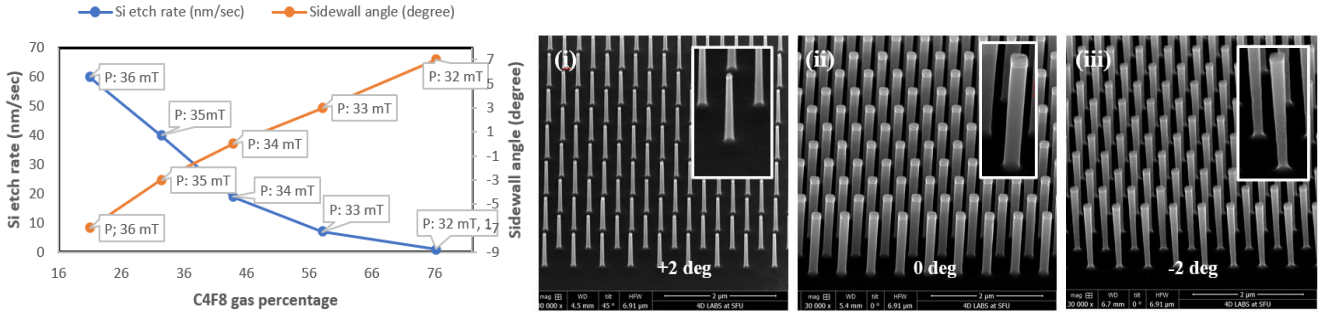
Changing the C4F8 flow rate percentage and chamber pressure allows us to tailor the sidewall angle to a required value depending on the application. For instance, to fabricate an atomic force microscopy probe, a large positively tapered profile is required. One application of nanostructures with a slight positive sidewall angle is that it will help facilitate the subsequent nanoimprint lithography process and demolding of a nanoimprinted replica from the silicon stamp.

Figure 3 shows the cross-sectional SEM image of two different HAR nanostructures using the etch process developed here, (a) 50nm nanowall with 500 nm pitch, and 2.5 um height (AR: 50), and (b) 150 nm nanowires with 500 nm pitch and 5.2 um height (AR: 35). Despite having such HAR nanostructures, the etch anisotropy remains unchanged resulting in vertical sidewalls.



(a) (b)

Figure 1 (a) The plot shows the Si etch rate and the sidewall roughness of nanostructures as a function of the chamber pressure in a dry etcher chamber; (b) SEM images that demonstrate reduced sidewall roughness when chamber pressure is increased from 20 mTorr to 35 mTorr at low temperature.



(a) (b)

Figure 2. (a) Plot showing the effect of the C4F8 flow rate percentage on the silicon etch rate and the sidewall angle in the non-switching etch recipe employed here; (b) SEM images demonstrate that decreasing C4F8 flow percentage leads to an increase of the sidewall tapered angle.

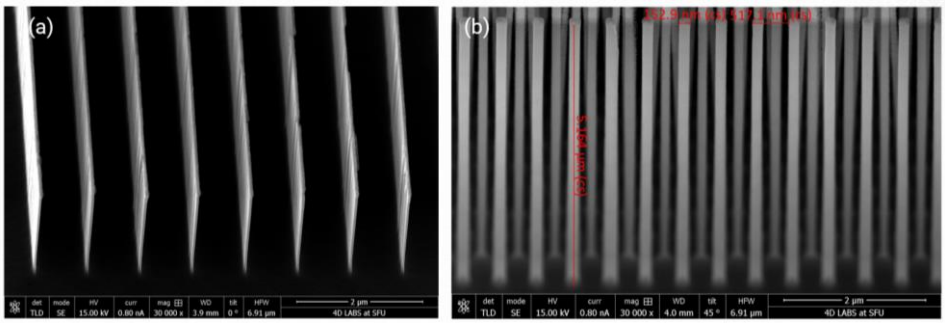


Figure 3. SEM images of (a) 50 nm nanowall with 500 nm pitch, and 2.5 um height (AR: 50); (b) 150nm nanowires with 500nm pitch and 5.2 um height (AR: 35).

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[i] Z. Liu, Y. Wu, B. Harteneck, and D. Olynick, *Nanotechnology*, **24**, 015305 (2013).

[ii] M. J. de Boer, J. G. E. Gardeniers, H. V. Jansen, E. Smulders, M. J. Glide, G. Roelofs, J. N. Sasserath, and M. Elwenspoek, *J. Microelectromech. Syst.*, **11**, 385 (2002).

[iii] T H Chung, H J Yoon, T S Kim and J K Lee; J. Phys. D: Appl. Phys. 29 (1996) 1014–1020.

[iv] Y. Lii and J. Jorn, *J. Electrochem. Soc.*, **137**, 3633 (1990).

[v] R. Abdolvand and F. Ayazi, *Sens. Actuators*, **A144**, 109 (2008).

[vi] B. Wu, A. Kumar, and S. Pamarthy, *J. Appl. Phys.*, **108**, 051101 (2010).

[vii] M. J. de Boer, J. G. E. Gardeniers, H. V. Jansen, E. Smulders, M. J. Glide, G. Roelofs, J. N. Sasserath, and M. Elwenspoek, J. Microelectromech. Syst. 11, 385 (2002).

[viii] F. Saffih, C. Con, A. Alshammari and M. Yavuz,, J. Vac. Sci. Technol. B, 32, 06FI04 (2014).

[ix] A. Ayari-Kanoun, F. Aydinoglu and B. Cui, J. Vac. Sci. Technol. B, 34, 06KD01 (2016).