Thermal scanning probe lithography (t-SPL) enabled high-resolution lift-off process

M. Käppeli, J. Chaaban, N. Hendricks, E. Çağın
Heidelberg Instruments Nano AG, Bändliweg 30, 8048 Zürich, Switzerland
myriam.kaeppeli@himt.ch

Thermal scanning probe lithography (t-SPL) is a lithography technique where a thermally sensitive resist (e.g. polyphtalaldehyde) is patterned by a heated tip integrated into a silicon MEMS cantilever. This same cantilever is equipped with a reader, which enables in-situ inspection of the patterned structures, ensuring high control over the resulting dimensions [Fig. 1]. The NanoFrazor t-SPL tool and its associated nanofabrication processes allow for the creation of nanoscale structures with a resolution in the 10s of nanometres[1]. The real-time reading capabilities of the NanoFrazor allow for high-accuracy alignment of the patterned designs to underlying structures, without the need for markers[2].

High-resolution (<100 nm) structures are useful for a variety of applications, such as creating artificial atoms, manipulating electronic properties (e.g. artificial bandgap), or creating metasurfaces for optical effects. A particularly timely application is in multiple-gate structures for quantum electronics, where the high resolution and the accurate alignment of multiple layers are crucial to device performance. For most of these types of applications, nanolithography with the NanoFrazor must be integrated into a process flow that includes a lift-off step[3].

High-resolution lift-off after t-SPL was demonstrated for structures as small as 20 nm[4] for non-repeating structures. Reaching such resolutions in a repeatable and consistent manner is critical, motivating the efforts to increase patterning endurance through optimizations to lithography parameters, thermal cantilever fabrication, and resist stacks. A further challenge in the high-resolution regime is the use of thin layers (<10 nm) of imaging resist on top of a multilayer lift-off stack [Fig. 2]. Defect-free and uniform coating of this stack and control of the process steps are needed for repeatable results.

In this talk, current results obtained using the high-resolution lift-off process developed in our laboratory will be presented. While resolutions of 15 nm line widths can be achieved during the patterning step, broadening during the resist stack opening to allow for lift-off results in resolution loss. Resolutions of approximately 20 nm in the resulting metal structures can be achieved with optimized processes. This talk will therefore include best practices regarding the handling of thin layers of resist and the use of t-SPL for high-resolution patterning over longer durations [Fig. 3]. The opportunities offered by using t-SPL to create such structures, such as the possibility to overlay high-resolution structures with existing ones with high accuracy, will also be discussed.

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[1] S.T. Howell *et al.*, Microsyst. Nanoeng., **6**, 21 (2020).
[2] M.C. Giordano et al., Adv. Mat. Interfaces, 2201408 (2022).
[3] M.C. Giordano *et al.*, Adv. Mat. Interfaces, **10**, 1 (2023).
[4] H. Wolf *et al.*, J. Vac. Sci. Technol. B 1 (2015)

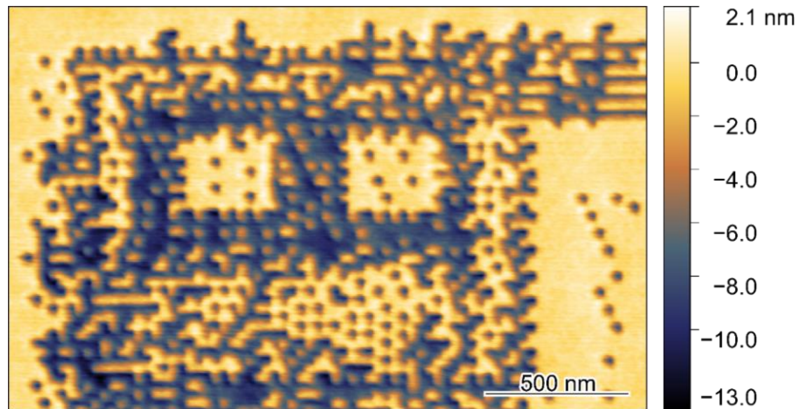

Figure 1: NanoFrazor-written pattern into a 10 nm thick PPA layer. The critical dimension is 30 nm, and the depth is ~8 nm.

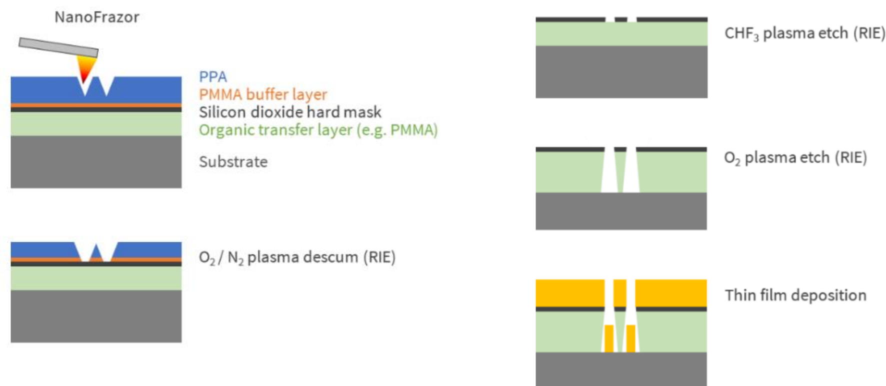

Figure 2: Process flow of high-resolution lift-off with the NanoFrazor.

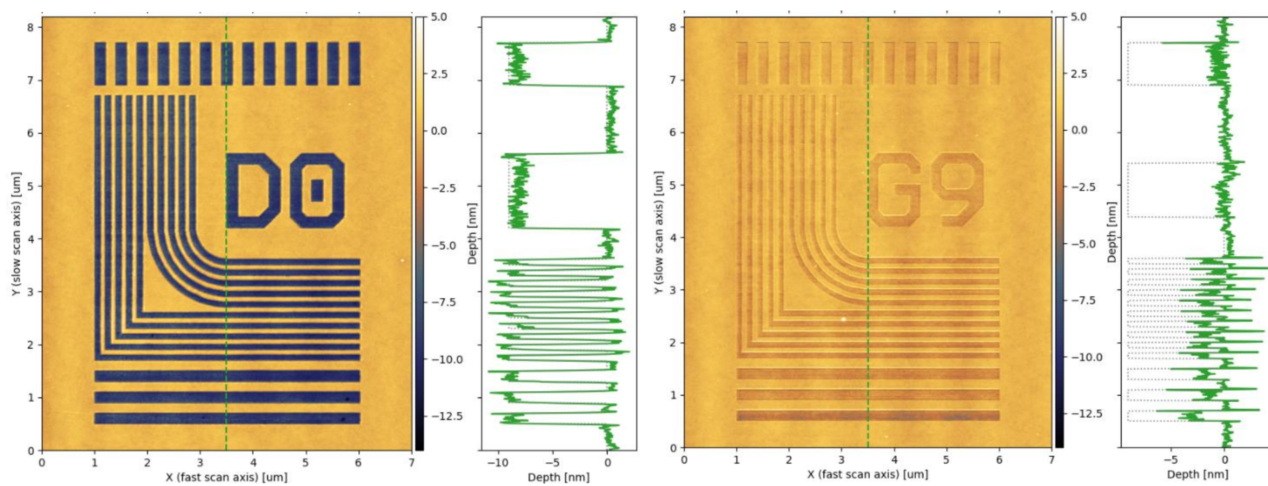

Figure 3: NanoFrazor-written patterns into a 10 nm thick layer of PPA, written with the same tip. Left: 31st pattern, ~10 nm deep. Right: 70th pattern, <5 nm deep.