Exploring electroluminescence and transport of color center light-emitting diodes as candidates for telecom quantum light sources

N. Ebadollahi[1,2], V.V. Kizhake[1,3], M.I. Davanco[1], K.A. Srinivasan[1] P.N. Namboodiri[1], A.M. Katzenmeyer[1], M. Pelton[3], J.M. Pomeroy[1]

[1]National Institute of Standards and Technology, Gaithersburg, MD 20899
[2]University of Maryland, College Park, MD 20742
[3]University of Maryland (Baltimore County), Baltimore, MD 21201
nikki.ebadollahi@nist.gov

The need for reliable quantum light sources drives our research to study color centers (CCs) in silicon as telecommunications O-band emitters. Building from photoluminescence (PL) measurements, we plan on comparing these emissions to electroluminescence (EL) measurements. To this end, we synthesized CC-embedded P-I-N junctions in silicon, creating CC light-emitting diode (CC-LED) devices. The two types of CCs synthesized were G-centers and W-centers, which show zero-phonon lines (ZPLs) at approximately 1269 nm and 1218 nm, respectively [1,2]. Here, we present our device design, fabrication process flow, and report on the device performance results from measurements to date.

To fabricate these devices, we first pattern and etch global alignment marks through the 220 nm silicon layer of a silicon-on-insulator (SOI) wafer. We then implant boron and phosphorous to synthesize p-doped and n-doped regions, respectively. Carbon (or silicon) is then implanted in the intrinsic region of the P-I-N junction to yield G- and W- centers, respectively. For our W-center wafer, we patterned and deposited Ti-Au metal contacts followed by a 250 °C anneal to enable CC activation. The G-center wafer requires a higher temperature anneal, therefore we anneal then pattern and deposit the metal contacts.

We vary the design parameters across our wafers containing 49 dies, each of which have 12 devices, to provide feedback for optimal EL emission. The CC implant area, wire width, and separation between p-type and n-type doped regions (Ohmics) are varied across the devices. Figure 1 shows the P-I-N junction of one of our devices, highlighting these design variables. To assess the effect of the presence of CCs on the device, we measure the I-V behavior, as shown in Figure 2, of two devices with the same design: a 9 μm^2 implant area, 5 μm wire width, and 3 μm gap between Ohmics. The only difference between the devices is that one has CCs while the other does not. The device with CCs has a higher resistance as the presence of defect centers presents a barrier to current flow. Also shown in Figure 2 are fits to the Shockley diode equation, $I = I_0[e^{\frac{qV}{nkT}} - 1]$. The CC implanted device shows a poorer ideality constant (n). In this talk, we will present the design and fabrication of our CC-LEDs, the LED characteristics, and EL measurements from the CCs at both room and cryogenic temperatures.

---

[1] Durand, A., *et al. Phys. Rev. Lett.* 126, 083602 (2021).
[2] Buckley, S.M., *et al.* Opt. Express 28, 16057-16072 (2020).

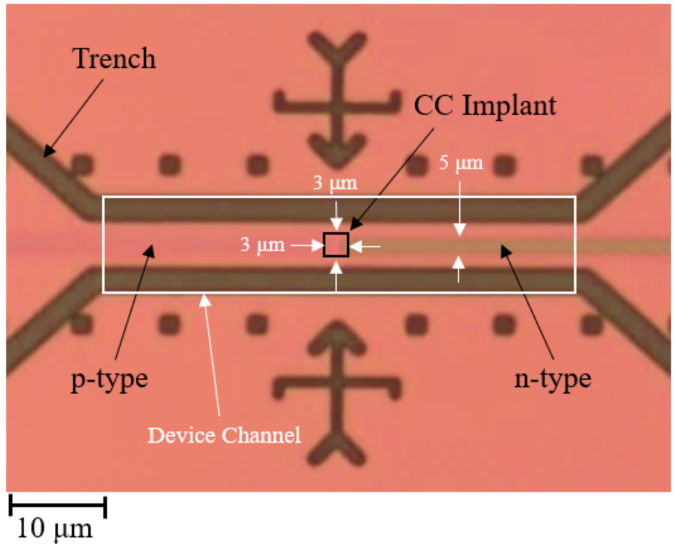

Fig 1. The micrograph shows the P-I-N junction of one of our devices. The black box indicates the CC implant area, the wire width is the width of the p- and n-type regions, and the separation between these is the distance between the two Ohmic regions. The device channel is contained within the white box.

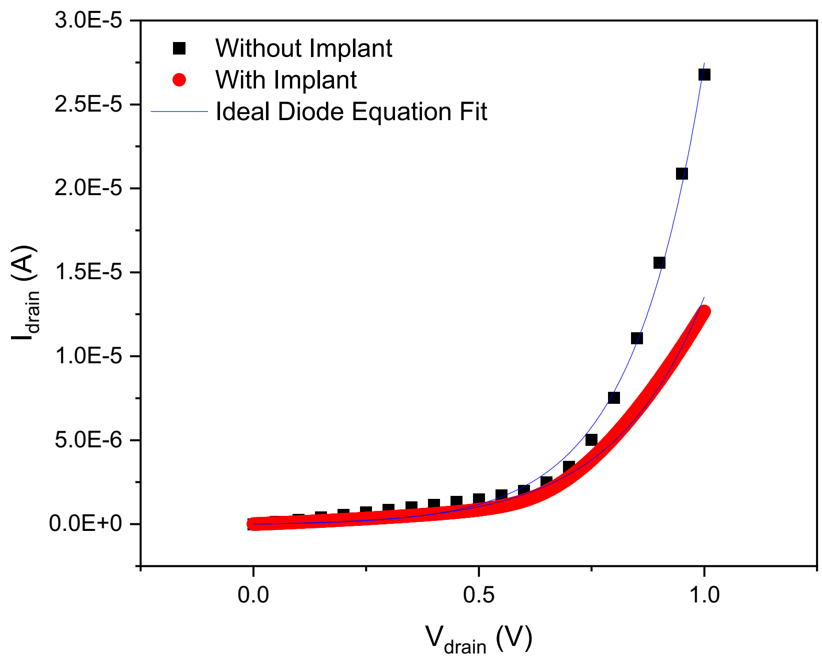

Fig 2. The graph shows a comparison between the I-V curves of a LED without (black) and with (red) color centers (CCs) implanted at room temperature from the same wafer and with the same dimensions. The data is fit to the Shockley non-ideal diode equation: $I = I_0[e^{\frac{qV}{nkT}} - 1]$ where I_0 is the saturation current, n is the ideality constant, q is the absolute value of electron charge, k is Boltzmann's constant, and T is temperature (K).