Robust and simplified gate design in surface-gated quantum dot devices for diagnostic qubits fabrication

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At the National Institute of Standards and Technology (NIST), our research is deeply engaged in the development of single gate layer MOS systems, specifically designed for surface-gated quantum dot devices. These systems are key to our mission of balancing design simplicity with functionality, especially for devices aimed at supporting qubits. Our primary goal is to achieve a very simple and robust design for quantum dot devices. By simplifying the gate design, we aim to reduce the likelihood of fabrication failures while ensuring these devices retain their ability to produce functional qubits and achieve higher device yields. The essence of our research lies in creating robust quantum dots that, despite offering limited control and less precise tuning of the electrostatic field, are still capable of generating qubits. While these qubits may not be fit for advanced applications such as quantum computing, they can be used as diagnostic qubits for material characterization.

Our current approach takes a step back from complex gate stack designs, that offer lots of freedom and control with complex process flow, which makes it easier to confine single electron with disadvantage of high possibility of failure. Instead, we focus on a simple and robust gate design that has less failure possibility. While these designs provide limited control and less precise tuning of the electrostatic field, they are still capable of producing qubits.

Figure 1 showcases previous single gate layer designs, setting the stage for our advancements in creating more compact gate structures. Our goal is to significantly reduce gate dimensions to improve single electron control and device efficiency, particularly important due to silicon's mass. This effort introduces a new gate design focused on enhancing barrier reliability by optimizing gate size and layout that are critical for better electron confinement and gate operation. An additional layer of complexity in our research involves addressing the challenges posed by low-temperature operations. To this end, we have been careful to design gate-to-ohmic connections that avoid acute angles, thereby reducing mechanical stress and potential field disturbances in environments reaching mere millikelvins.

Moreover, our research includes a thorough exploration of the effects of different gate shapes on field dynamics. We hypothesize that the use of rectangular gates might lead to the creation of dual barriers, a concept that holds intriguing potential for quantum dot functionality. Conversely, gates with sharp endpoints are expected to create narrower traps, offering a different set of advantages for electron confinement. These hypotheses and their associated designs are illustrated in Figure 2. The exploration of these gate shapes can potentially have practical implications for enhancing the performance and functionality of quantum dot devices.

In this talk, we will discuss how we evolve from previous generation designs towards quantum dot devices with simpler, more robust architectures. This approach aims to decrease failure rates for these qubits utilizing simpler process flow and gate design.

(a) (b)

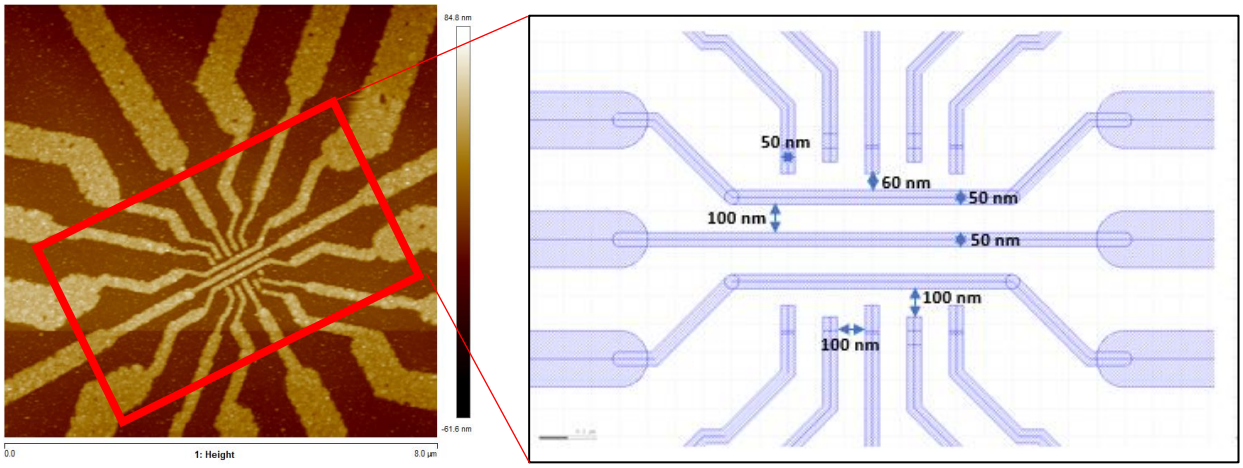

Figure 1. (a) The AFM image of the fabricated device illustrates the gate layout design through lithography is shown in the figure above. Sketch (b) shows the CAD design of the fabricated gate layout including dimensions.

(a) (b)

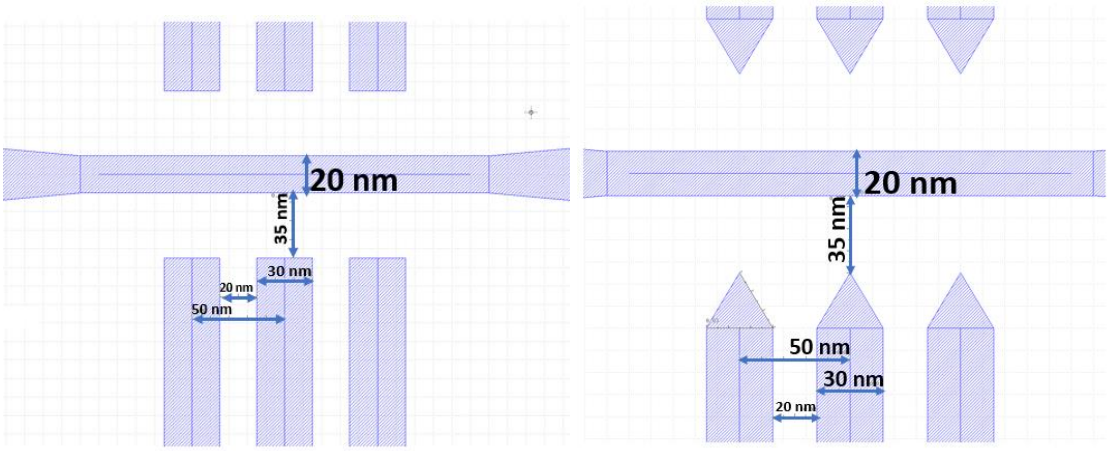

Figure 2: Examples of CAD design of the new generation of gate layout structure with more simple design is shown in the sketches above. Sketch (a) illustrates the new and simple gate layout design with smaller dimensions. Sketch (b) illustrates the gate layout design with shaper endpoints are expected to create narrower traps.