Next generation fabrication techniques for top gated qubits in silicon

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Many groups around the world are adapting conventional semiconductor manufacturing technology to fabricate top gated qubits in a variety of silicon-based systems. Currently, the highest precision devices are fabricated using direct-write e-beam lithography [1], but they are still characterized by significant relative line edge roughness and gate width uncertainties leading to overhead regarding tuning multi-qubit devices. For example, simulation results suggest a factor of 2 difference in tunnel splitting between 70 and 72 nm wide gates. In this work, we present two methods for improving the precision of gate definition and fabrication: direct write patterning for dopants [2], and nanoimprint templating for ultra-precise 3D structures. [3]

First, we describe a 3-D geometry using bipolar patterned dopant delta layers as both fixed confinement regions and tunable gate electrodes (see fig. 1A), similar to what has previously been shown for 2-D bipolar devices (see fig. 1B). With a patterning precision of 0.7 nm on Si(100), gates can be fabricated with arbitrary separation. However, a separation of below approximately 5 nm for 2-D electrodes in silicon without additional dielectric material results in an effective short between electrodes. The bipolar regime is thus invoked to increase the barrier height between gate electrodes, thus allowing tighter packing of features. While this architecture has been shown on stacks of SOI or Si-Si/Ge-Si with less precise pattering steps, [4] this work will focus on single layer bipolar patterning on silicon.

Secondly, we describe a method to create nanoimprint templates that can create conventional aluminum top gates with a precision down to a few nanometers and line edge roughness of approximately 1 nm, as shown in Figure 2. In contrast to the direct write technique which will require arrays of tips operating simultaneously to produce the approximately 10^6 qubits to achieve flexible quantum supremacy, the step and flash technique of nanoimprint lithography points to a direction of highly parallel systems with unprecedented large-scale precision. [5]

References:

[1] Kruit et al, Ultramicrocscopy, 164, 31-45 (2016)
[2] Keizer et al, ACS Nano, 9, 12537-12541 (2015)
[3] Ballard et al, JVST B, 32, 021805 (2014)
[4] Sigillito et al, Applied Physics Letters, 120, 190401 (2022)
[5] Resnick et al, Materials Today, 8 (2), 34-42 (2005)

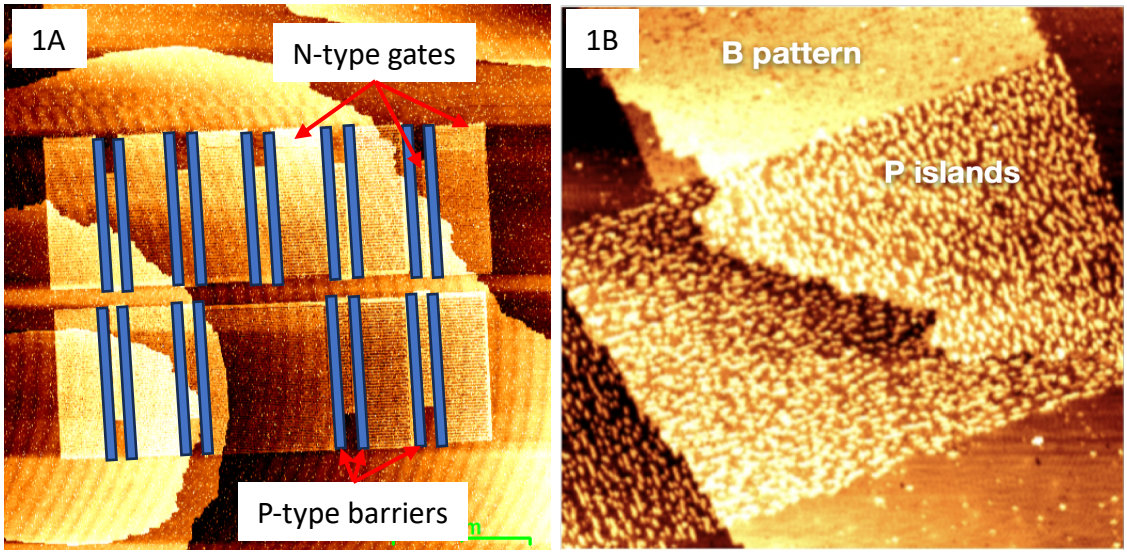

Figure 1: Concept for a bipolar system as architecture for a top gated qubit. 1A: A schematic of a pattern for a top gated qubit. Patterns for phosphorus gates have been pre-patterned. To prevent inter-gate tunneling, boron will be placed as barriers.1B: STM image of an area patterned to be a delta layer of phosphorus (center) as well as a subsequent pattern prepared for boron deposition (top). Note the tolerance of 0 nm between the patterns.

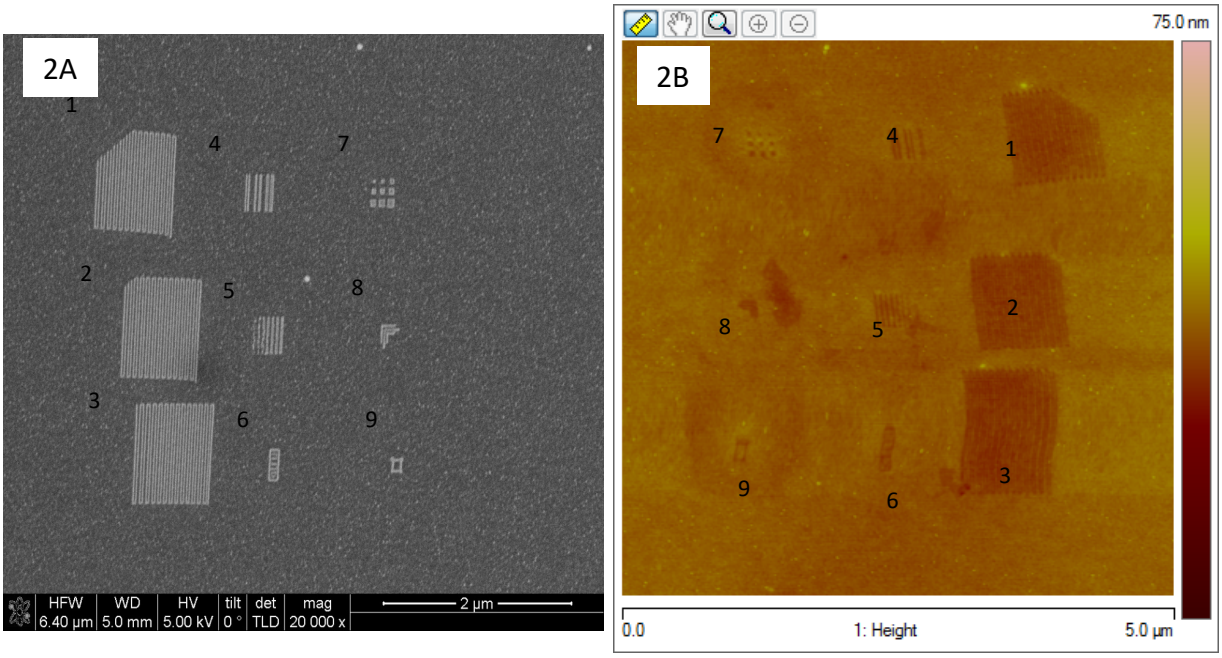

Figure 2: Comparison of etched and imprinted images. Figure 2A: SEM image of test patterns after silicon patterning, selective ALD, and etching. Figure 2B: atomic force microscopy image of a hardened nanoimprint resist after printing with the sample in figure 2A. Note the mirror imaging. Patterns on the left and right are numbered.