Passive Tuning of Photonic Integrated Circuits by Automated Silicon Ion Implantation

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The demands for drastically increasing computing power combined with the imminent end of transistor scaling have been the main drivers for research into alternate computing paradigms. Integrated photonics as a promising platform for neuromorphic computing, mixed-precision accelerators, and quantum computing\ has garnered heavy attention recently in academia as well as industry.

Nevertheless, a key challenge in upscaling integrated photonic systems is the sensitive nature of the components to fabrication imperfections. Since photonic circuits are usually designed to operate in the analogue domain, standard process variations in etching rate, exposure parameters, and chemical mechanical polishing conditions adversely affect their functionality. Prominent techniques correct for these imperfections via active phase shifters such as thermo-optic heaters consuming a significant portion of the power budget.

Here[1], we demonstrate a flexible method for passively tuning silicon nitride photonic circuits at scale using automated silicon ion implantation via marker search and alignment as shown in Figure 1. We obtain controlled and stable shifts in the optical properties without the need for any active elements. We performed a detailed material study using scanning transmission electron microscopy (STEM) and conducted electron energy loss spectroscopy (EELS) analysis to understand the fundamental changes occurring at the atomic scale. Leveraging these advances, for the first time, we demonstrate passively aligned energy-efficient photonic circuits enabling applications in wavelength addressable memory and a photonic computing engine exploiting wavelength division multiplexing.

[1] Varri, A., Taheriniya, S., Brückerhoff-Plückelmann, F., Bente, I., Farmakidis, N., Bernhardt, D., Rösner, H., Kruth, M., Nadzeyka, A., Richter, T., Wright, C. D., Bhaskaran, H., Wilde, G., Pernice, W. H., Scalable Non-Volatile Tuning of Photonic Computational Memories by Automated Silicon Ion Implantation. Adv. Mater. 2023, 2310596. https://doi.org/10.1002/adma.202310596

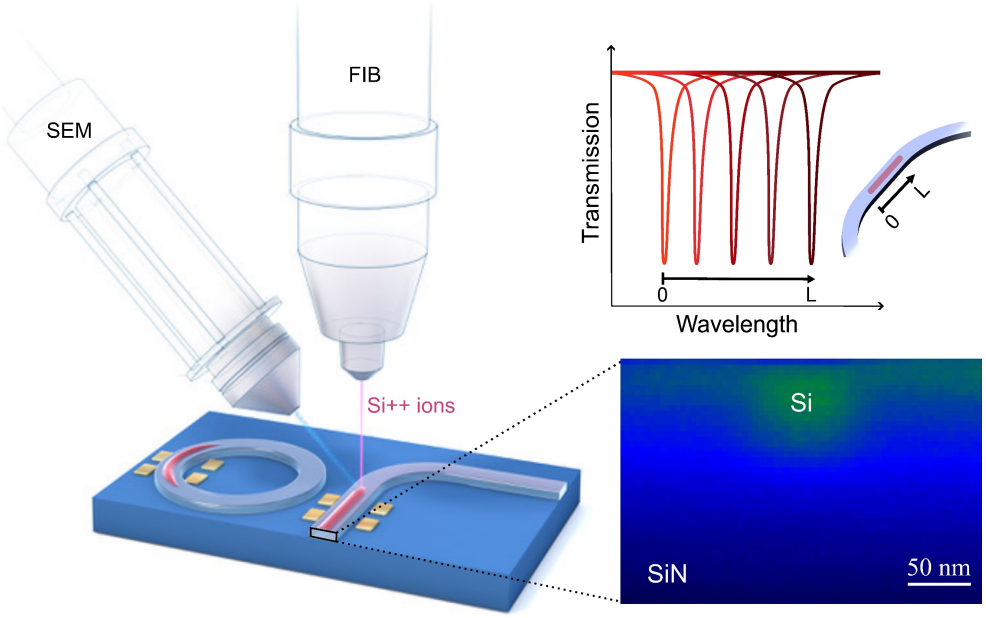

Figure 1: Photonic device tuning by automatized silicon implantation. (a) Silicon ion patterning on photonic circuits using the Raith VELION focused ion beam. The photonic circuits consist of silicon nitride ring resonators on top of the SiO_2 substrate. The ions are directly written into the waveguide without requiring a mask. The inset on the right displays the plasmon map reconstructed from low loss energy spectrum. The patterning process leads to silicon ion implantation in the Si_3N_4 waveguides. (b) Schematic of the optical response. Redshifts in the transmission spectrum of ring resonators with larger pattern lengths confirm the increase in the effective refractive index of the waveguide material.