In-house 20k memristor/CMOS monolithic integration and its statistical characterization

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Interest in memristor devices (or resistive switches or RRAM) has seen a rapid rise in the past decade due to their electronic programmability, non-volatile state storage with years-long retention and small two-terminal footprint [1]. New types of memristor devices based on novel designs and material stacks are constantly being researched and developed in academic facilities. These academic efforts require in-house integration with separately fabricated foundry CMOS before being suitable for larger scale testing, prototyping of hardware neural networks and harvesting a large set of experimental data suitable for comprehensive device modeling. Hybrid CMOS/memristor circuitry enables integrated functional electronics in a monolithic chip design [2], supporting easy access for the CMOS circuit. However, foundry tape-outs in this hybrid technology are limited and expensive [3], and require a significant infrastructure for the circuit design, integration, and testing. In this work, we integrated 20,000 memristor devices onto a commercial 3.3 V, 180 nm 6-metal layer complementary metal-oxide-semiconductor (CMOS) chip to demonstrate the performance of a large population of devices [4].

The compatibility of memristive devices with CMOS circuits is limited by the high forming and switching voltages of the memristor devices [5]. One effective way to lower the forming voltage is to use a thinner oxide layer [5], [6]. In Fig. 1.a., single devices with four different thicknesses (15 nm, 20 nm, 25 nm, and 30 nm) of the TiO_{2-x} layer are investigated to find a suitable forming voltage. These results help us integrate CMOS-compatible memristor devices with a 97% yield for forming and an 85% yield for switching where the ON/OFF ratio > 10 (Fig. 2). The measurement parameters are optimized to achieve a high ON/OFF ratio and endurance via the design of experiments (DOE) using the Latin square approach [7]. The Latin square approach allows the utilization of only 16 tests to study a domain normally requiring 256 tests. Fig 2.b. shows the statistics of the forming, set, and reset voltage of 1000 integrated devices. The device shows promising endurance and a large separation between the high resistant state (HRS) and low resistant state (LRS) (Fig. 3.a,b,c). The device-to-device variabilities and devices Set/Reset current separation are also shown in Fig. 3.d,e. This work demonstrates the high performance of these monolithically-integrated memristors across a large population and the potential for development of larger arrays in the future.

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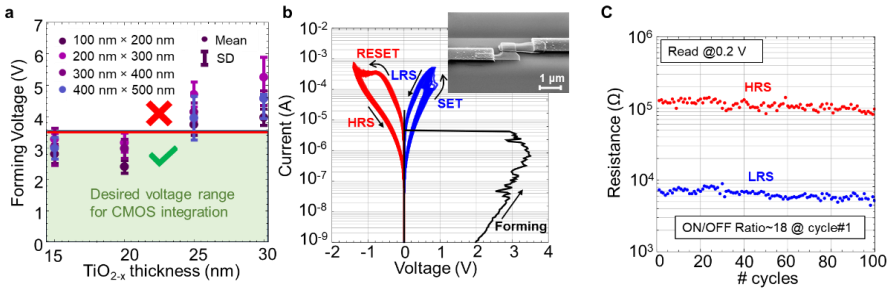

Figure 1: Standalone device on silicon substrate, a) the relationship between the forming voltage and oxide thickness for 4 different sizes of devices b) current vs. voltage characteristic of 100 switching cycles for 15 nm TiO_{2-x} thickness with ~ 400 nm × 500 nm device size; c) High resistance state (HRS) and low resistance state (LRS) for 100 switching cycles.

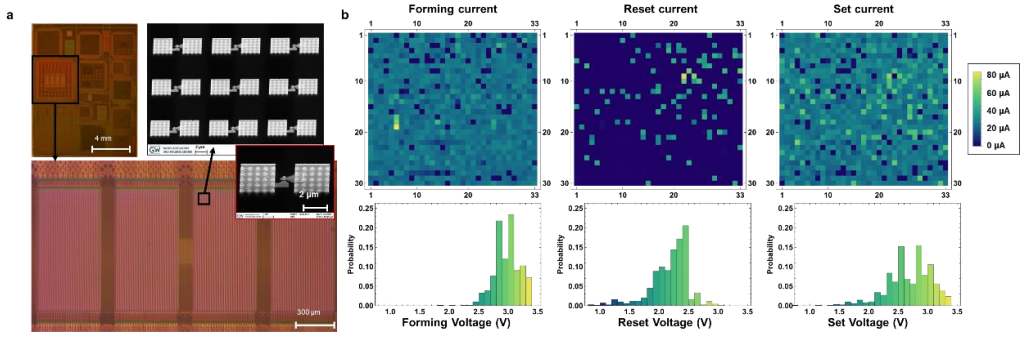

Figure 2: a) Chip with integrated 20,000 memristor devices, b) (above) Current map of 1000 devices for 15 nm TiO_{2-x} thickness with ~ 100 nm × 200 nm device size. (below) histograms showing the distributions for the devices.

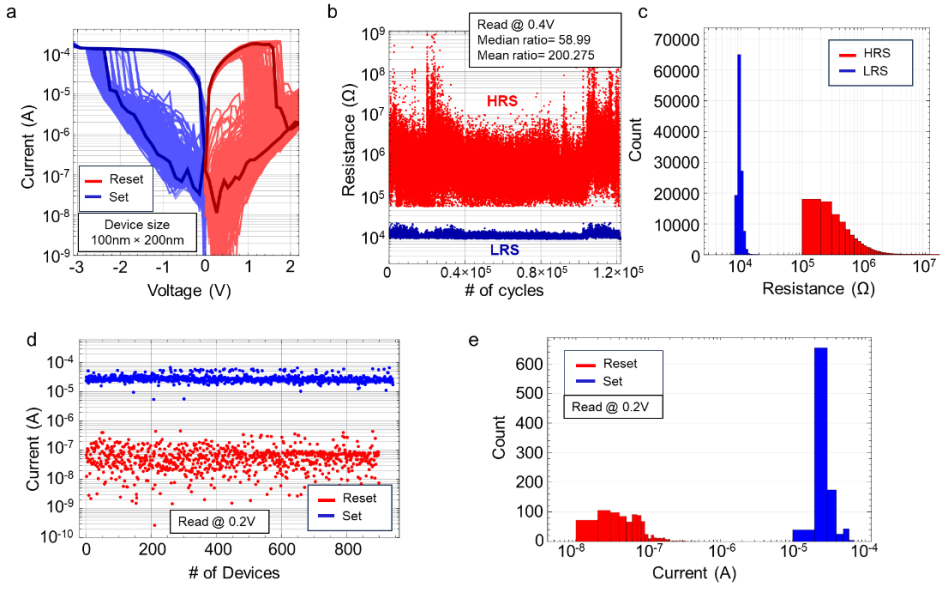

Figure 3: a) Current-voltage characteristics for 200 cycles of a 100 nm × 200 nm device, b) Device endurance of 100 nm × 200 nm device size, c) histogram plotting of HRS and LRS resistances. Device-to-device variabilities for 1000 devices, each device size 100 nm × 200 nm d) resulting set and reset currents and e) histogram of the distribution of set and reset currents.