Field-Emission Scanning Probe Lithography-Based Mix and Match Fabrication of Junctionless FETs

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In the last decades, there has been a significant escalation in merging semiconductor nanowires (NWs) with nanoelectronics and nanoelectromechanical systems (NEMS).[1] In the field of nanoelectronics and nanomechanics, Si NWs have a crucial impact due to their wide-ranging and versatile transduction capacities in sensing and actuation.[2] Allowing a resolution in single-digit nanometers by diminishing the proximity effects using low-energy electrons, field-emission scanning probe lithography (FE-SPL) is a cost-efficient nanopatterning method.[3,4] Allowing direct imaging after patterning with the same cantilever, FE-SPL-based mix-and-match method is utilized for the fabrication of Si NW-based junctionless field effect transistors (JLFETs), Figure 1. JLFETs are fabricated on an SOI fragment consisting of a 12-nm-thick Si layer with a 9-15 Ω.cm resistivity with <100> surface orientation and 25 nm buried-oxide layer (BOX) settled on a Si handle layer. The method contains both micro-scale fabrication, to create source, drain, gate electrodes, and nano-scale fabrication, to fabricate Si NW. Photolithography, Figure 2a, and reactive-ion-etching (RIE), Figure 2b, are utilized to pattern micro-scale structures for nano-scale patterning, conducted by FE-SPL, Figure 2c. Different dimensions for the NW and gate lengths and widths are specified to observe different characteristics for varying dimensions of the JLFET structure. Positive tone nanopatterns are utilized on the ultra-thin Si layer by cryogenic RIE, Figure 2d, achieving cryogenic temperatures aimed at obtaining vertical side walls with a low etching rate. Isolating the microstructures with NW, Figure 3, behavior of JLFET is characterized with IV measurements. Applying different gate voltages (V_G), current change on the NW (I_D) is monitored, Figure 4, shows the linear regime operation of the device where the average channel conductance is 3 μS. Thus this study provides a fabrication method utilizing mix-and-match patterning based-on FE-SPL under ambient conditions and electrical characterization for JLFET.

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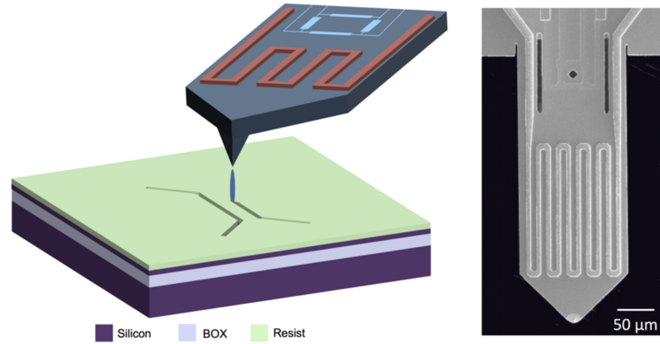

Figure 1: FE-SPL: Working principle of the FE-SPL (Left) and SEM image of the cantilever with piezoresistive sensor and thermal actuator (Right).

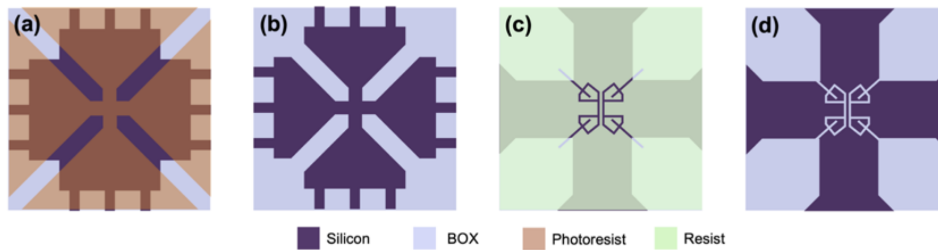

Figure 2: Mix-and-match fabrication process flow: a) Photolithography, b) RIE, c) FE-SPL, and d) Cryogenic RIE.

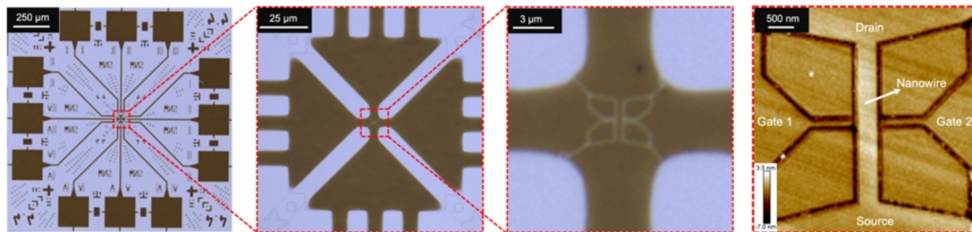

Figure 3: JLFET structure: Confocal images of contact pads, gate, drain, and source areas and JLFET structure after cryogenic etching. AFM image of components of the JLFET (Right).

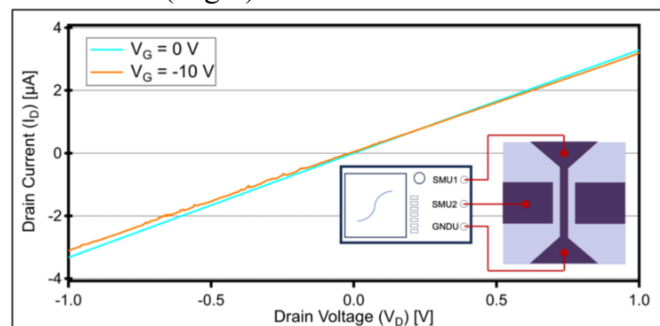

Figure 4: Electrical characterization: Setup for electrical characterization of the JLFET and drain current-voltage plot for the gate voltages values of 0 and -10 V.