A WSe_2-MoS_2 JFET with tunable polarity via back gate voltage control

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Junction field effect transistors (JFETs) are essential building blocks in electronic circuits due to their simplified structure design, which eases the fabrication process and potentially reduces manufacturing costs[1]. The control of current flow between the source and drain is achieved by directly depleting the charges in the channel, while the suppression of leakage current through the gate is facilitated by the junction formed by the channel and the gate. This minimizes the necessity for a gate dielectric, and therefore, JFET often exhibits better high-frequency performance compared to traditional MOSFET counterparts.

Van der Waals integration introduces a novel approach to forming high-quality p-n junction, which is crucial for the operations of JFETs[2]. In this work, the p-n junction formed by WSe2-MoS2 through vdW integration is harnessed, and a WSe_2-MoS_2 JFET with tunable polarity is demonstrated. Figure 1. shows a) the optical image of the WSe_2-MoS_2 JFET and b) the schematic of the cross-section of the WSe_2-MoS_2 JFET. The MoS_2 serves as the gate, controlling the carrier concentration in the WSe_2 channel, thereby regulating the current flow between the source and the drain. A universal back gate is introduced to modify the polarity of the device. Figure 2. illustrates the effect of back gating. With a carefully chosen back gate voltage, our JFET functions as an NFET under positive V_{bg}, while under negative V_{bg}, it can also function as a PFET. The ambipolar transfer characteristics of WSe2 contribute to the realization of polarity switching[3]. Figure 3. highlights the quality of the p-n junction formed by WSe_2 and MoS_2. The device shows minimal leakage current from the gate in comparison to the current flow in the channel. In conclusion, this work realizes the switching of polarity in JFETs and provides greater flexibility for future circuit applications.

[1] Lim, J.Y., Kim, M., Jeong, Y. *et al.* Van der Waals junction field effect transistors with both n- and p-channel transition metal dichalcogenides. *npj 2D Mater Appl* **2**, 37 (2018).
[2] Lee, CH., Lee, GH., van der Zande, A. *et al.* Atomically thin p–n junctions with van der Waals heterointerfaces. *Nature Nanotech* **9**, 676–681 (2014).
[3] Wang, Z., Li, Q., Chen, Y. *et al.* The ambipolar transport behavior of WSe_2 transistors and its analogue circuits. *NPG Asia Mater* **10**, 703–712 (2018).

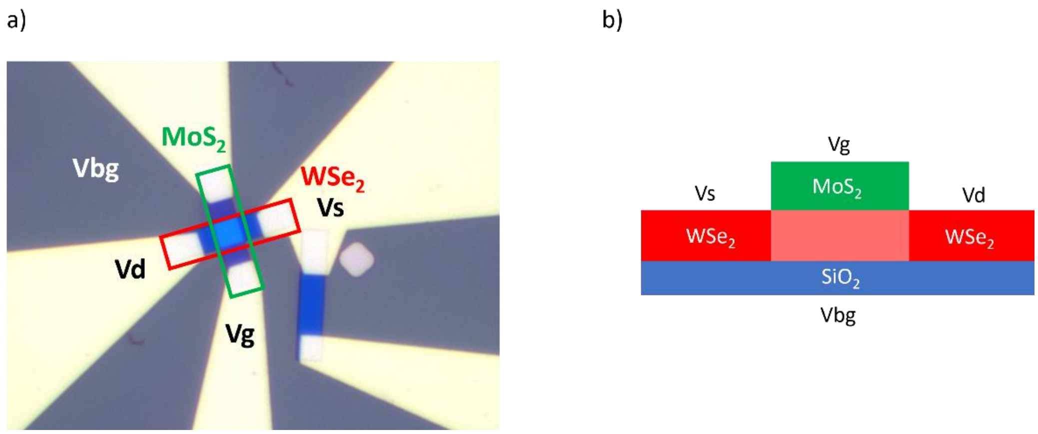

Figure 1: a) The optical image of the WSe_2-MoS_2 JFET. MoS_2 is used as a controlling gate for the WSe_2 channel with minimal leakage through WSe_2-MoS_2 heterojunction. b) Schematic of the cross-section of the WSe_2-MoS_2 JFET.

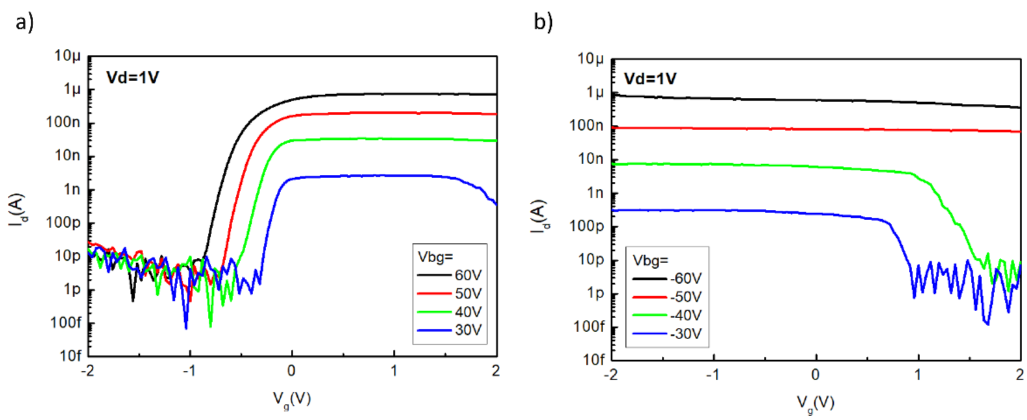

Figure 2: The polarity of the WSe_2-MoS_2 JFET being tuned by the back gate voltage. a) Device under positive back gate voltage functions as a NFET b) Device under negative back gate voltage functions as a PFET.

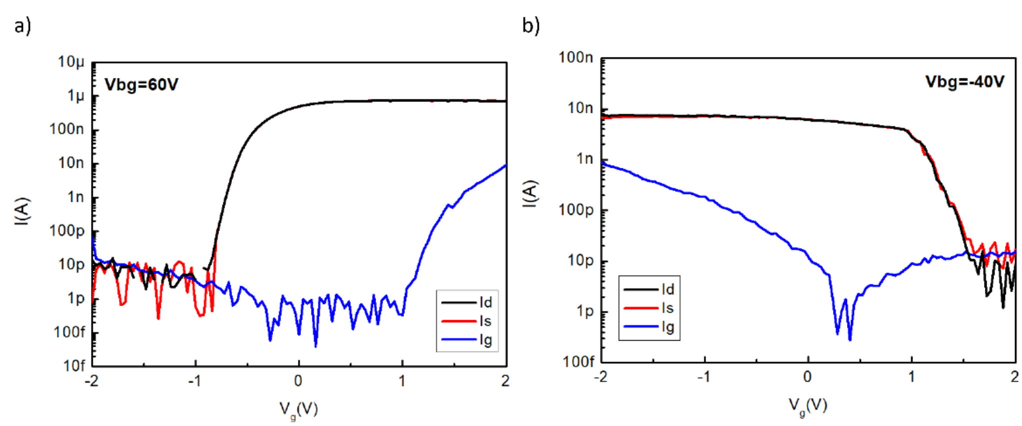

Figure 3: Leakage current through WSe_2-MoS_2 heterojunction is negligible under the region of operation for both a) NFET and b) PFET.