Full-Wafer Nanoimprint Patterning for CMOS Pilot Line Development and Manufacturing

Matthew C. Traub, Myriam Willegems, Steve Smout, Pau Guell I Grau, Silvia Lenci, Mohamed Saib, Eleonora Storace, Aurelie Humbert, Bogumila Kutrzeba Kotowska, Igor Turvets*, Joey Hung*

imec, Kapeldreef 75, 3001 Leuven, Belgium
*Nova LTD, 5 David Fikes St., Rehovot 7632805, Israel

The introduction of full-wafer nanoimprint lithography (NIL) patterning to existing CMOS production lines offers the potential for cost-effective production of new flat optics, biosensors, and many other devices. Nanoimprint provides single-step fabrication of 3D geometries over large areas, while advanced 300 mm semiconductor tools provide high-performance inorganic materials and process precision and repeatability for high-volume manufacturing. However, the effective marriage of NIL and CMOS capability requires the development of a novel set of fabrication processes and metrology while simultaneously adapting existing NIL processes and materials to comply with CMOS contamination rules. In this talk, we will present our results on our on-going incorporation of NIL into imec's advanced 300 mm pilot line, focusing on the case of full wafer patterning of high-refractive index glass for AR waveguide combiners and flat optics.

By encapsulating 1.9 refractive index glass in silicon nitride which is closely index matched to the substrate, we are able to process high-index glass in our 300 mm pilot line and access CMOS tooling for processing and metrology. The fabrication of NIL masters with DUV steppers allows the patterning of 300 mm substrates with features down to 60 nm critical dimension without the contamination risk of exposing glass materials to immersion tools. High-selectivity direct etching into silicon nitride was developed using commercially available NIL resins and a fully-patterned 300 mm NIL master with variable pitch gratings. To monitor feature fidelity and uniformity during the patterning process, an optical critical dimension model was built for multiple pitch features and applied to full wafer imprints, providing detailed insight into the uniformity of the replication. Together, these results demonstrate the expanded potential for NIL in a precision CMOS environment.

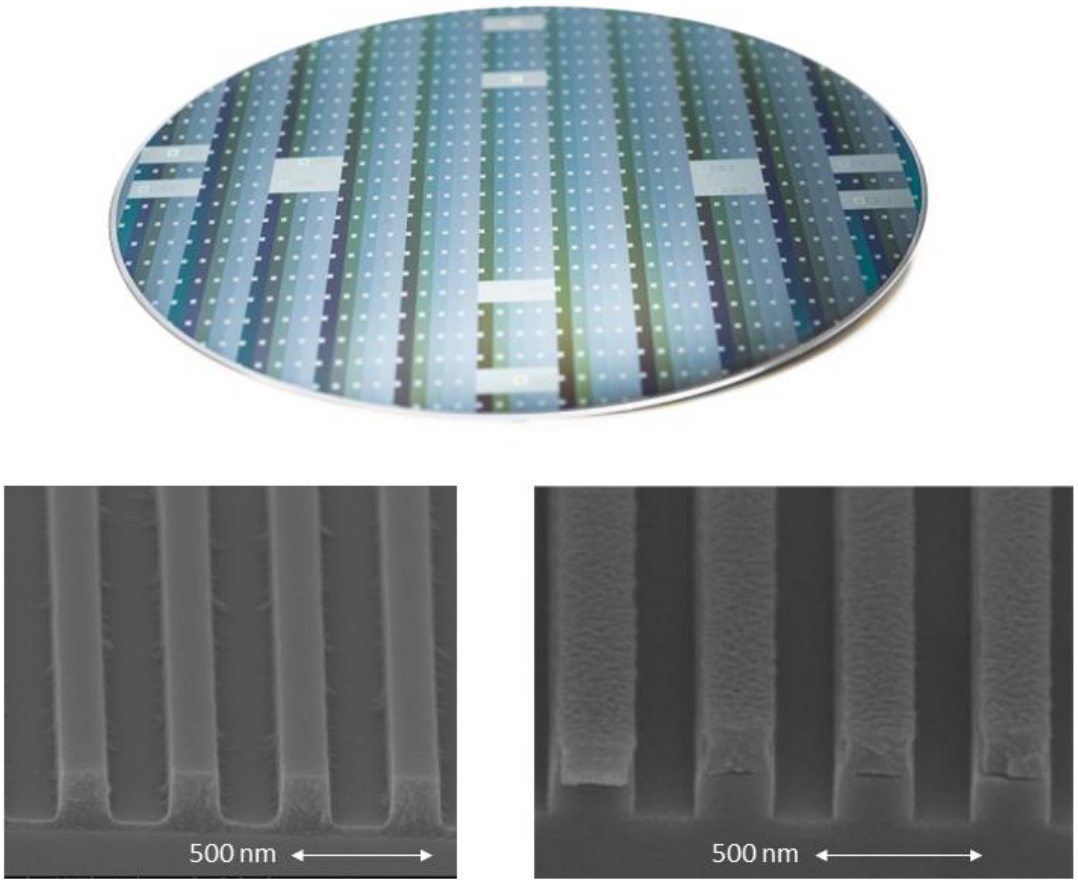

Figure 1. Top: A 300 mm nanoimprint master manufactured by immersion DUV at imec, fully patterned with gratings ranging from 400-800 nm in pitch. Bottom left: Nanoimprint replicated 400 nm pitch structure on silicon nitride on a 300 mm silicon substrate. Bottom right: Etching of gratings into silicon nitride on a 300 mm glass substrate through a NIL resin mask, prior to resist stripping.