

# Automation of Pattern Driven Metrology for Photonic Devices Utilizing a FESEM for Process Monitoring

C.M. Eichfeld, B. Liu, M. LaBella, G.P. Lavalley  
*Materials Research Institute, The Pennsylvania State University, University  
Park, PA 16802*

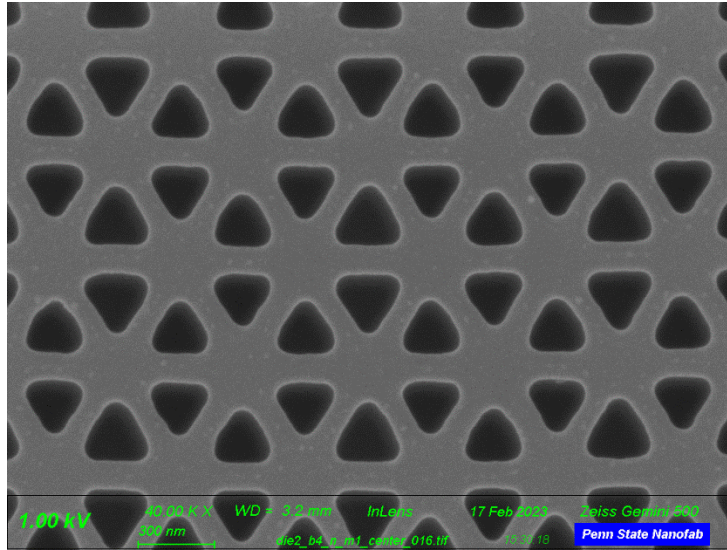
M. Zai  
*GenISys Inc., P.O. Box 410956, San Francisco, 94141-0956*

K. Gieb, S. Bauerdick  
*GenISys GmbH, Eschenstr. 66, 82024 Taufkirchen (Munich), Germany*

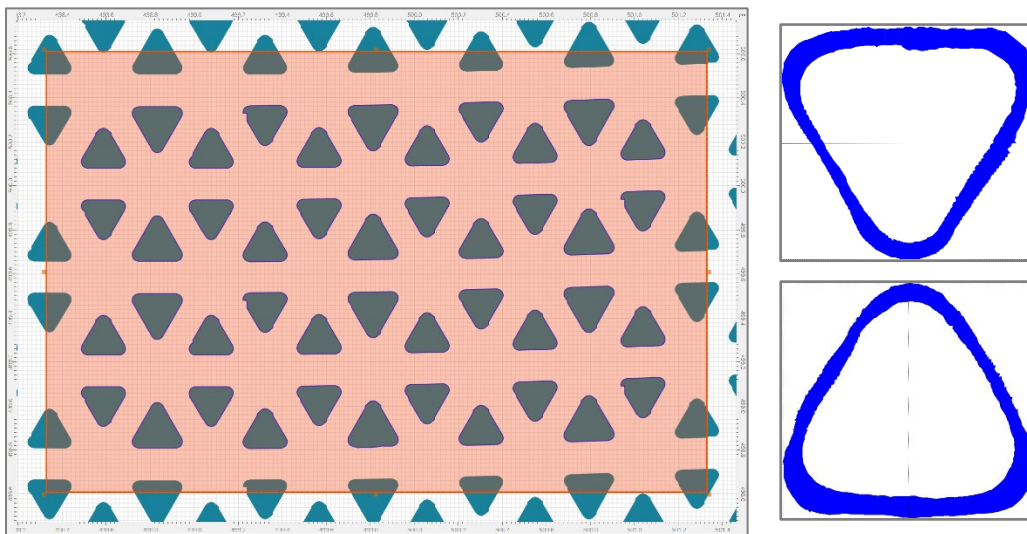
There is a growing need for automated nanostructure characterization and process monitoring in R&D institutions. Purpose built CDSEM's are great for mass production but can be less flexible and more costly to acquire and operate than laboratory type versatile SEM's that already exist. In this paper we present methods and results for utilizing our FESEM (Zeiss Gemini) to acquire pattern driven automated images in combination with measurements using an integrated software upgrade kit for metrology (GenISys InSPEC). A special focus is on use cases with photonic devices (Fig. 1) like large area gratings, photonic crystals, meta lenses, etc.

In this paper we will discuss challenges and present solutions related to acquiring and analyzing images using an automated flow. This needs to be both easy (no manual coding) and resilient to real world limitations. These could be related to the tool hardware such as positional drift, stage accuracy, and focus control or to imaging artifacts and pattern deviations.

We will focus on several examples related to projects that span from process calibration to process monitoring. We develop go/no-go criteria-based customer driven specifications for devices and corroborate FESEM based measurements with device performance data to further justify results. We utilize tools for process monitoring such as thresholds, shape fitting/ comparison, or PV bands (process variation, Fig. 2) to identify when a process is out of specification.



*Figure 1:* Example of one SEM micrograph taken as part of a larger photonic device structure etched into the silicon device layer of a silicon-on-insulator (SOI) wafer.



*Figure 2:* Layout-based contour extraction and measurements as defined in the software user interface (left) for one scan region and resulting PV bands (right) for the detected features from the corresponding SEM scan.