Multi-channel testing systems for efficient prototyping of emerging memory devices and arrays

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The recent artificial intelligence (AI) boom has brought significant advancements across various applications. However, challenges remain in the energy efficiency of AI hardware. Emerging memory devices provide promising solutions to address such challenges. Non-volatile memory devices and crossbar arrays are widely used in in-memory computing chips, accelerating neural networks through parallel vector-matrix multiplication[1], [2]. While various resistive switching devices have been utilized to build emerging hardware, there remains a critical need for research on emerging materials and devices to improve device performance metrics, such as endurance, stability, yield, *etc.,* for industry-level integration[3].

One challenge in developing emerging materials and devices is testing the performance of new devices within in-memory computing systems. Unlike single-device characterization, evaluating emerging devices within in-memory computing systems requires highly parallel analog inputs and output reading for multiple channels, flexible configuring for various device arrays, and computing capability for fast algorithm prototyping. Designing and iterating on-chip peripherals to meet these requirements for different devices and applications is time-consuming and unrealistic.

This presentation introduces our multi-channel testing systems with parallel analog inputs and readout peripherals for fast prototyping emerging devices within in-memory computing systems. The system implementations include customized printed circuit boards (PCBs) for different encoding methods (e.g., pulse amplitude or width) of analog inputs and parallel analog-to-digital conversions. Additional computing functions are developed in software to accommodate various computing methods for algorithm prototyping. The systems are designed to be reconfigurable for emerging device arrays with different dimensions. Results will demonstrate the use of the systems in reading and programming the memristor conductance in one-transistor-one-memristor (1T1R) crossbar arrays with the dimension of 128×64.

References

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