Semiconductor Traceability: Die Annotations Patterning by Maskless Exposure Technology

G. Oakes[1], K. Varga[1], T. Uhrmann[1], R. Holly[1], T. Zenger[1], A. Spitzer[1], F. Bögelsack[1]
S. Vanclooster[2], M. Reybrouck[2], D. Janssen[2], N. Van Herck[2], M. Vandevyvere[2]

[1] EV Group, DI Erich Thallner Strasse 1, St. Florian am Inn, Austria
[2] Fujifilm Electronic Materials (Europe) N.V. Zwijndrecht, Belgium

Abstract— **The semiconductor traceability is becoming an important subject concerning the overall manufacturing processes, ranging from FEOL, BEOL and packaging processes. The newly developed software "die annotation" feature represents a novel method for the applications in advanced packaging. By applying high resolution dielectrics, the patterned DataMatrix codes down to 200µm×200 µm were resolved by maskless exposure technology.**

I. Introduction

The fabrication of FO WLP encounters several process challenges, like warpage of the reconstituted wafers occurring due to application of different materials for RDLs, dielectric layers, or silicon/mold blend and their different thermal expansion properties. The die shift is critical for patterning and redistribution of layers, when die stacking is required in 3D heterogenous integration.

The RDL must be reliably connected, as these are the fundamental interconnections that otherwise lead to blocking between the PCB and chips [1]. Application of mask–based lithography is facing some limitations. The steppers show difficulties copping with inaccuracies from die placement and die shift variations. The given reticle size and optics dimensions of static exposure systems limit the exposure area. This is challenging in large die interposer fabrications, where stich–lines and or mismatches overlap regions of reticle exposure field can affect the electrical properties within the RDL.

The dynamic pattering capabilities of the maskless exposure lithography solves challenges in interconnect formation processes. The technology employs dynamic alignment modes with an automatic focus, to adapt to the substrate material and surface variations. The advanced distortion relates and analyses real–time data from visible or near-infrared topside and backside alignment. It accomplishes this by actively compensating for mechanical die placement, stress induced inaccuracies such as rotation, displacement, expansion, and high-order distortions of the substrate [1].

II. Methodology

Maskless Exposure was employed for patterning of the RDL and vias. Process evaluation and optimization is very efficient, e.g., combination of DoE can be conducted on just one wafer. By extending the lithography process windows, various processes conditions were explored to improve the resolution of vias and the dielectric layers. Low–temperature cure polyimide dielectric material (FujiFilm Electronic Materials LTC9320–E76B, negative tone) was investigated. The high throughput dielectric polyimide was particularly developed to meet the requirements of the complex FO WLP [3].

III. Results

The film thicknesses, soft bake temperatures, exposure wavelength, dose, and matrix of focus position and post–exposure bake (PEB) were varied. An exposure matrix using both wavelengths in a single and step–less combination was adjusted in the process flow, with exposure doses ranging from 50 mJcm^{-2} to 1125 mJcm^{-2}, with a step size of 25 mJcm^{-2}. The focus was evaluated in advance on dummy wafers to investigate the influence of the exposure dose and the respective wavelength sensitivity on the resolution. The resolution results are shown in Fig. 1. This experiment was performed on bare Si wafers with the dielectric material.

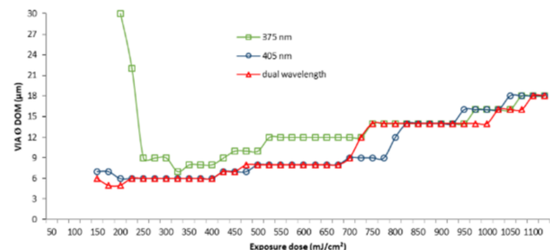

Fig. 1. Resolution results across exposure dose and exposure wavelength matrix for LTC9320–E76B, on Si with softbake 100 °C, SB FT 10µm and spray development

Exposure at 375nm, the typically available i–line closest laser wavelength, delivers slightly lower resolution behavior and a smaller process window. For comparison intentions, both 405nm wavelength and dual–wavelength exposure, where both wavelengths were utilized simultaneously. The resolution in the latter two exposures shows better resolution than 375nm. The process window also displays a resolution from a top aperture of 6 µm, with a post–soft bake layer thickness of 10 µm.

One of the characterization methods is SEM inspection. Fig. 2 displays a selection of cross-sections fabricated on dummy Si substrates with negative tone polyimide dielectric. The through–hole plating resolution was optimized to 2.0µm - 3.0µm. The patterning enables a reduction of the FT to 7 µm. Additional DoE will be carried out to investigate the dependencies of dielectric layers under various reflow requirements.

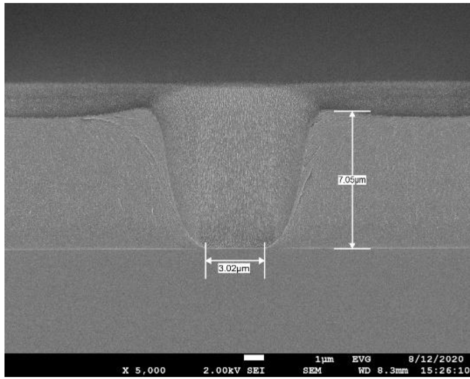

Fig. 2. SEM profiles showing high–resolution profiles

The optical microscopy of the DataMatrix codes patterned by dielectris in two various film thickness (after SB) ranges: 7.5 and 15 µm was performed. Min. readable codes for the film thickness 7.5 µm (after SB) was 200×200 µm (Fig. 3) while min. readable codes for 15 µm FT (after SB) was 400×400 µm.

By these results, the suitability of this developed traceability method for the annotations of the large size dies in advanced packaging is proven.

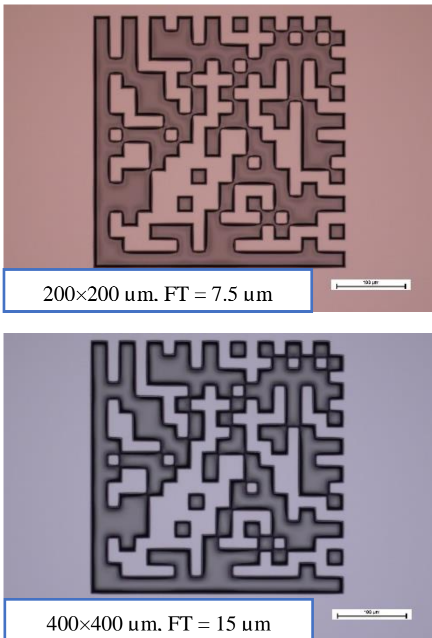

Fig. 3. Min. readable codes for the film thickness 7.5 µm (after SB) was 200×200 µm while min. readable codes for 15 µm FT (after SB) was 400×400 µm.

In the present investigation, high–resolution patterning performance in terms of achieved feature sizes and sidewall profiles was proven. Maskless exposure sustains heterogeneous integration processes by patterning the low–temperature cure polyimides dielectrics making the technology eligible for ultra–high density (>4 RDL layers) FO WLP patterning. The unique software features of maskless exposure technology, the dynamic die annotation enable patterning of QR codes, data matrix, bar codes on every single chip/die contributing to traceability efforts in semiconductor industry.

References

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