Nanoimprinting-induced strain engineering of MoS2-based field effect transistors fabricated by stencil lithography

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Stencil lithography (SL) is a fabrication method used to modulate the surface of a substrate, relying on the aperture of a shadow mask to allow the flow of atoms, molecules, or particles for deposition or etching[1]. Due to its non-resist processing and reusability, SL has a wide range of applications, such as gratings for solar cells, fabricating transistors on non-planar substrates, and electrodes connected with two-dimensional (2D) materials. Although this method has been applied to fabricate electrical contacts with 2D materials, previous reports mainly focus on planar substrates and do not take into account the bombardment of 2D materials during the evaporation process[2]. Here, we propose a non-vacuum fabrication of a nickel thin-film (a few micrometers thick) as a stencil mask to deposit metal electrodes on patterned dielectric substrates. This is done first, followed by the transfer of 2D materials on top of the electrodes to avoid deposited bombardment and any surface adsorbents from conventional photolithography. Simultaneously, this method can be utilized to fabricate shadow masks to define the channel area of 2D materials-based bottom-gate transistors with large-scale arrays using an etching method, which also avoids polymer contamination from photolithography.

Figure 1 schematically demonstrates the fabrication of gold electrodes on the grating groove substrate through this method. **Figure 1a** shows patterned photoresist created on the Indium Tin Oxide (ITO) glass substrate by mask aligner photolithography. The resist is used as a mask for deposition of nickel stencil mask on the exposed area of ITO glass and a nickel stencil mask is obtained on the glass substrate after removing residual photoresist. **Figure 1d** demonstrates the nickel stencil mask is peeled off from the ITO glass, and then this mask is attached to the target substrate for transferring pattern of mask on the attached substrate. **Figure 1e** shows target materials' layer is covered on the surface of stencil mask and aperture area of target substrate. **Figure 1f** exhibits that the expected patterns of electrodes are defined on top of patterned substrate. **Figure 2a** illustrates the scanning electron microscopy (SEM) image of developed photoresist (PR) pattern. **Figure 2b** shows the feature size of free-standing nickel mask, and the width of gap can be slightly controlled by modulating thickness of stencil mask. **Figure 2c** shows that a defined gold electrodes is transferred from nickel stencil mask after thermal evaporation, and electrodes outline is conformally followed the outfit of stencil mask. While as shown in **Figure 2d**, conventional fabricated electrodes typically has a warping edge. **Figure 3a and 3b** are optical images of fabricated nickel stencil mask for deposition and etching respectively. **Figure 3c** shows MoS_2-based FETs on the patterned grating, and **Figure 3d** gives etching MoS2-arrays pattern on the patterned substrate without introducing photoresist contaminations.

[1] Du, Ke, et al. "Stencil lithography for scalable micro-and nanomanufacturing." Micromachines 8.4 (2017): 131.

[2] Bao, Wenzhong, et al. "Lithography-free fabrication of high quality substrate-supported and freestanding graphene devices." Nano Research 3 (2010): 98-102.

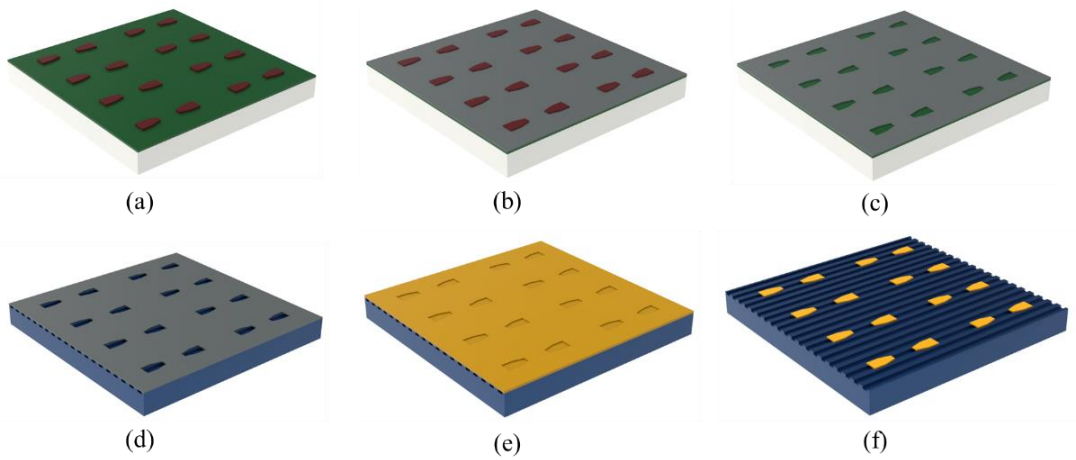

Figure 1. Schematic process of the proposed non-vacuum fabricated stencil mask and definition of electrodes on patterned substrate.

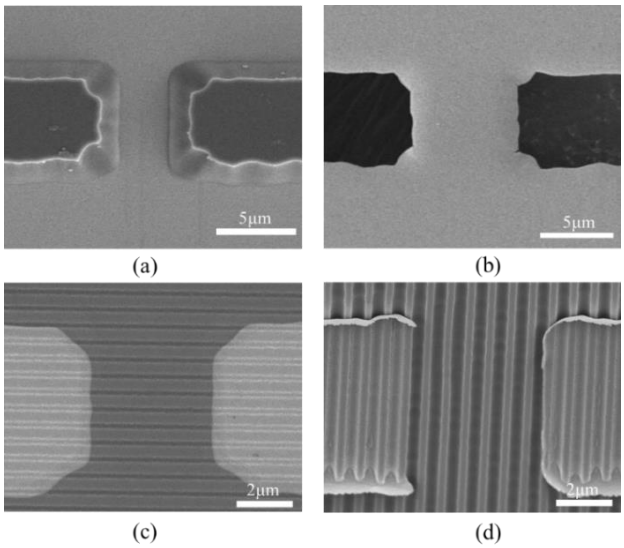

Figure 2. SEM images of each step morphology of sample and conventional fabricated method of defining electrode on the patterned substrate.

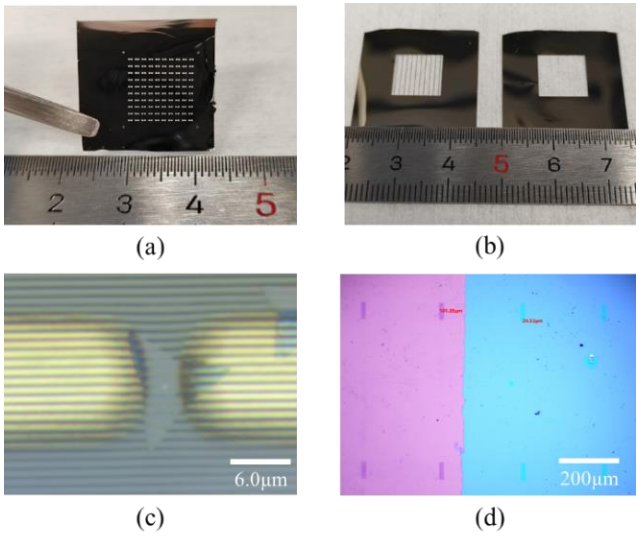

Figure 3. Optical images of fabricated stencil mask and defining pattern on the substrate.