Neural Networks Implemented on Memristive SoC chip for Prompt Detection of Heart Attack

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Myocardial infarction (MI), commonly known as the heart attack, stands as a prevalent global health threat. Despite the time-sensitive nature of heart attack treatment, current MI detection technologies suffer from delays and imprecision, leading to a limited ability to identify and address heart attack incidents within the critical rescue timeframe. We have previously proposed and demonstrated an innovative approach to enhance the prompt and accurate detection of heart attacks, leveraging plasmon-enhanced Raman spectroscopy with collapsible nanofinger and in-memory computing (IMC) through deep learning. That proof-of-principle demonstration was implemented in a relatively small memristor array (128x64) driven by peripheral circuits on a large set of PCB boards. To make the entire system portable for practical applications, much large neural networks on a fully integrated system on chip (SoC) are needed, which have been achieved in this study. Our design is characterized by low latency, high accuracy, and energy efficiency thanks to a lightweight multilayer perceptron (MLP) and its end-to-end execution on a memristor based SoC with ten 256x256 crossbar arrays and other necessary components, such as on-chip processor. Our research highlights the potential of memristive IMC hardware in accelerating machine learning to address current limitations in medical diagnostics.

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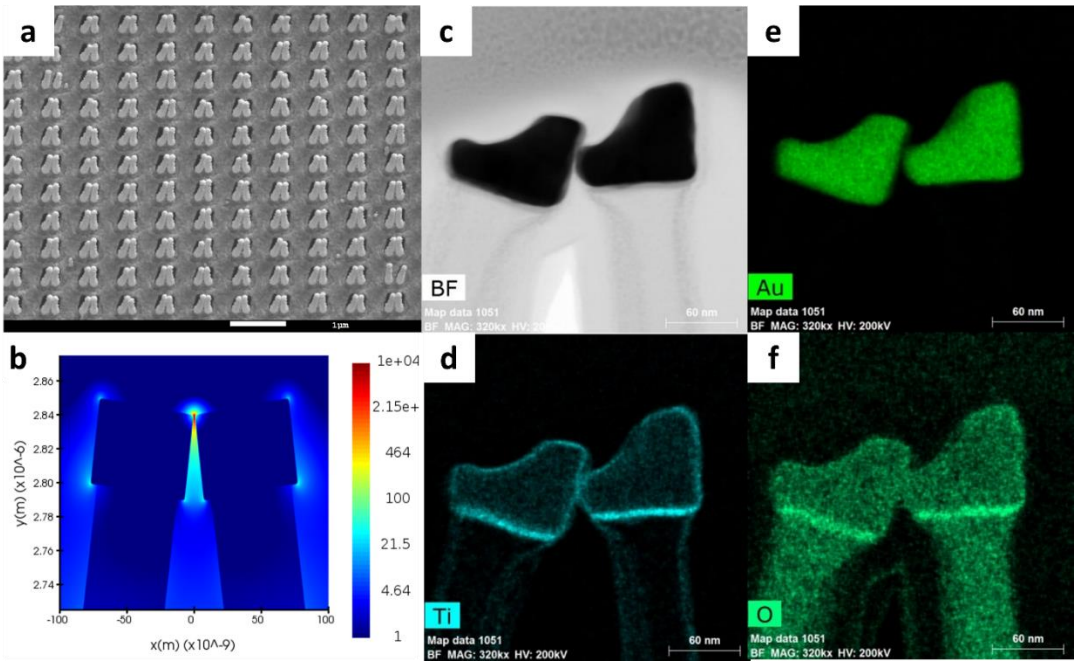

Figure 1. (a) SEM image of nanofingers after collapse. (b) Numerical Simulation of the electrical field enhancement of collapsed nanofinger. (c) TEM image of the nanogap in the nanofingers. (d-e-f) EDS mapping of Ti, Au, and O in the TEM image, respectively.

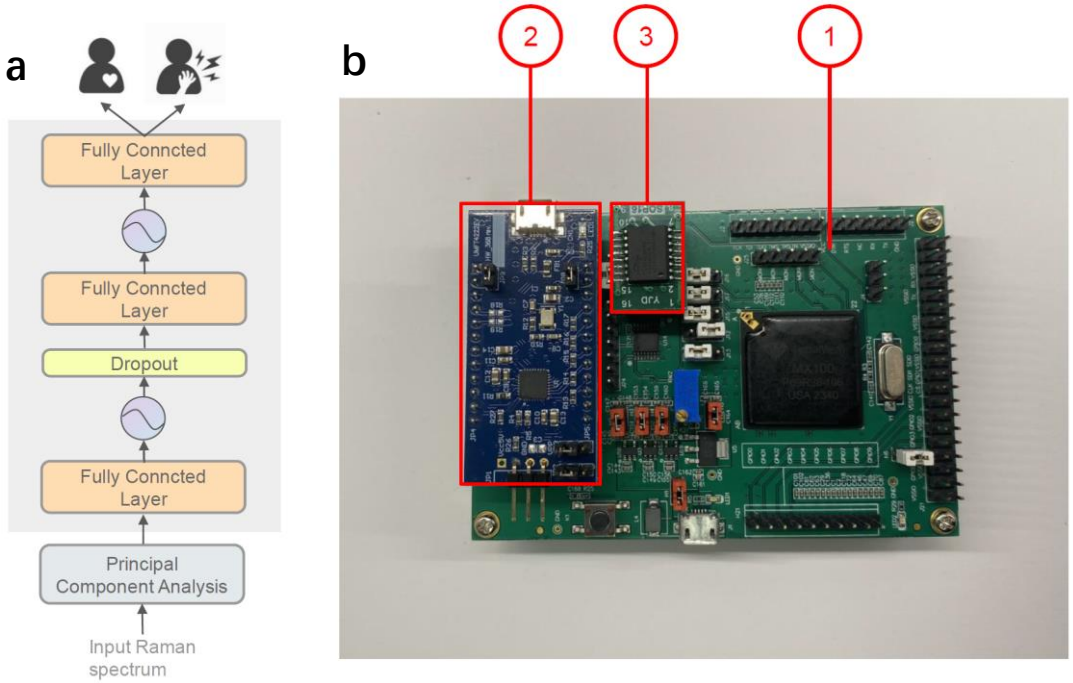

Figure 2. (a) The framework of neural networks implemented on Memristive SoC chip for prompt detection of heart attack. Our framework integrates three fully connected (FC) layers for efficient feature learning and classification. Inference results indicate an individual's susceptibility to a heart attack. (b). Our Memristive SoC chip, which is an evaluation board with attached USB 2.0 to QuadSPI bridge and SPI flash. Part 1 is The MX100 evaluation board contains the MX100 SoC. Part 2 is the USB 2.0 to QuadSPI bridge connects the SPI port on the evaluation board to the USB port on ourcontrol host. Part 3 is the SPI flash provides additional memory for bootup or storing input/output data.