# Fabrication of Microstructure Devices on Porous Nanolattice Films

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In recent years, there has been an exponential decrease in integrated circuit (IC) dimensions, resulting in significant challenges in the control and manufacturing of electronic devices with precisely controlled electrical properties. One critical issue is the need for materials with low dielectric constant, which can be used to reduce delays in high density ICs [1]. Such materials can be made from nanoporous materials, which can have degraded stiffness at low density due to their random porosity [2]. One potential candidate is nanolattices, which can have high stiffness and low optical refractive index [3]. Another area that can benefit from nanolattice materials is integrated photonics in areas such as virtual reality (VR) and augmented reality (AR) devices. These devices utilize integrated photonics like diffractive optics, waveguides, and metasurfaces to direct light onto the glass surface to overlay digital content onto observed objects. The critical aspect of the design is the incorporation of low-refractive nanolattice materials, which can improve the index contrast resulting in more effective light trapping, modulation, and manipulation [4]. However, little work exists on the fabrication of microstructures such as micro electrodes and waveguides on the nanolattice, which is challenging due to the difference in length scale and multilayer processing on porous layer.

In this research, we have developed a method to pattern microscale features onto the porous nanolattice layer using a shadow evaporation and colloidal phase lithography. That goal of this work is to create micro-electrodes to measure the capacitance value and characterize the dielectric constant of the device. The proposed process is shown in Figure 1, where the silicon wafer is patterned with closely packed microparticles with a diameter of 0.5 μm over a resist height of 800 nm. Then the samples are exposed to a lithography process using a 325 nm laser with 90 $\mathrm{mJ/cm^2}$ dose, creating the resist template as shown in Fig. 1(a). After development, the samples undergo atomic layer deposition (ALD), where they are coated with $Al_2O_3$ using trimethyl aluminum and water as precursors. The film was deposited with 200 cycles to achieve a conformal coating with 22 nm thick shells, as shown in Fig. 2(b). Next, a resist layer is applied over the nanolattice layer to planarize and protect the underlying structures. On top of the flattened layer, 200 nm thick $TiO_2$ layer is deposited through a shadow mask using electron beam evaporation to create a “dog-bone” geometry. Then the resist template is removed from the nanolattice structure through a thermal desorption at 550 degrees in the furnace.

The SEM images of the fabricated mono-nanolattice layer of particles and deposited $TiO_2$ “dog-bone” shape layer is shown in Figure 2(a) and (b), respectively. Figure 2(c) shows the SEM image of the structure of the fabricated nanolattice layer away from the dog bone structure. Microcracks with nanolattices underneath are visible in the sample, as shown in Figure 2(d), because of thermal-induced mechanical stress, which will be invested further. We aim to present a thorough overview of the fabrication process for nanolattices with various microstructure geometries. The presentation will emphasize the challenges and variations observed during the processing of microstructures on nanolattices and offer detailed insights into the methodology.

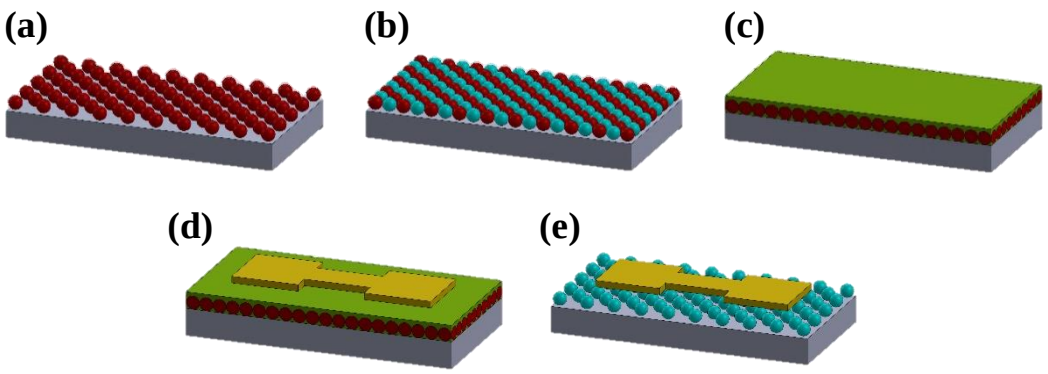


***Figure 1.*** *Fabrication process of the nanolattice structure (a) photoresist 3D nanostructures (b) ALD (c) planarization (d) deposit of* $TiO_2$ *dog bone layer (e) thermal cycle to remove resist*

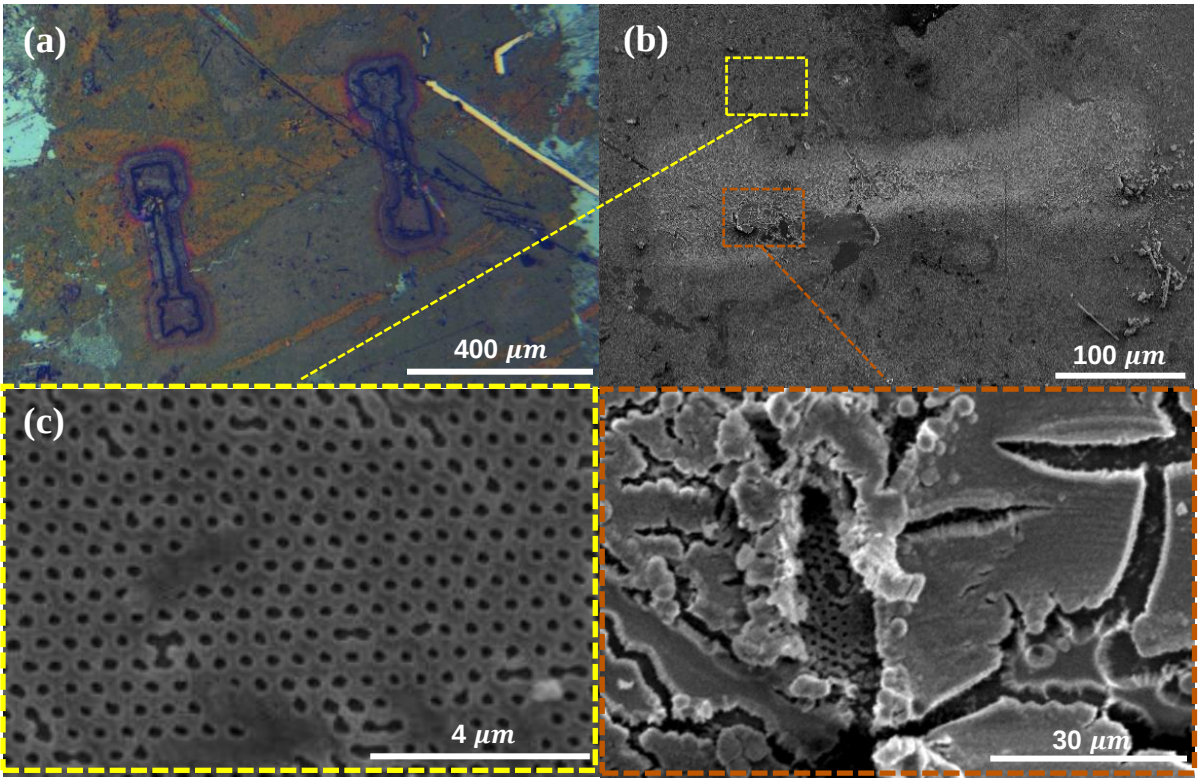


***Figure 2.*** *Top-down images of the 200 nm thick* $TiO_2$ *"dog bone" layer on nanolattices from (a) optical microscope and (b) SEM. Zoomed in area of the area showing the (c) nanolattice holes and (d) nanolattice below the cracked* $TiO_2$ *film.*

**Reference**

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