Vertical Trench Etching by Repetitive Dry and Wet Anisotropic Etching and 3D Self-aligned Sidewall Nano-patterning

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3D stacking of nano-devices is an efficient way to increase areal density where further downscaling of lateral device dimension runs against fundamental, practical, or economical limits. A good example of this approach is in V-NAND or 3D-NAND memory systems[1], where stacking is achieved mainly by employing plasma processing. Plasma etching features was previously used as a template for self-aligned mask formation using so-called edge and corner lithography, after which sidewall features can be formed by crystallographic etching techniques[2,3]. To explore smaller length scales in self-aligned sidewall patterning, the feature size and shape must be better defined, which has been investigated in this work by incorporating crystallographic wet etching in the trench formation process. The repetitive combination of dry and wet etching has been reported before for nanowire formation[4], but not on the sub 200 nm scale or for sub 20 nm sidewall patterning as demonstrated in this work.

Nanometer-sized line patterns are formed wafer-scale on (100) Si substrates by displacement Talbot lithography, and an iteration of dry and wet etching steps is used to create vertically stacked wedge type structures at the sidewalls of the trenches defined by (111) surfaces (Fig. 1 and 2). In this method, a thin SiO_2 hard mask of ~4 nm is sufficient for this process. The concave corners of the vertically stacked trenches are further processed in a self-aligned manner (Fig. 3). Corner lithography is applied to protect all concave corners followed by thermal oxidation to protect all {111} planes. The concave corners are made accessible for further processing by timed etching of the Si_3N_4 layer. Local sidewall nano patterning is demonstrated by creating diamond-like cavities after etching through the opened concave corners in KOH etchant (Fig. 4). The thus created new sharp corners and edges form templates for the self-aligned device fabrication.

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[1] Shim et al., Trends and future challenges of 3D NAND flash memory, IEEE International Memory Workshop, Monterey, CA, USA, 2023.

[2] Westerik et al., Sidewall patterning – a new wafer-scale method for accurate patterning of vertical silicon structures, J. Micromech. Microeng. 28, 015008 (2018).

[3] Ni et al., Wafer-scale 3D shaping of high aspect ratio structures by multistep plasma etching and corner lithography. Microsyst Nanoeng 6, 25 (2020).

[4] He et al., Novel fabrication for vertically stacked inverted triangular and diamond-shaped silicon nanowires on (100) single crystal silicon wafer, J. Micromech. Microeng. 30, 015003 (2020).

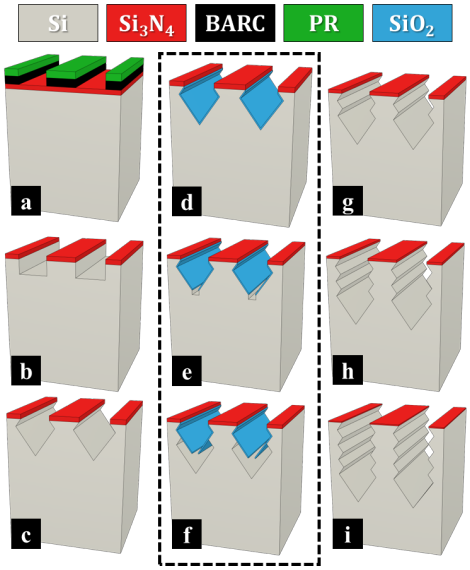

Figure 1: Schematic process flow of vertically stacked 3D nanostructures in (100) silicon. PR/BARC line patterning a) is followed by mixed mode RIE, resist strip b) and timed anisotropic silicon etching in KOH c). Iteration steps (indicated by a dashed box) consist of thermal oxidation d), directional RIE etching of SiO_2 e), and KOH etching f). SiO_2 hard mask stripping in HF g). Vertically stacked nanostructures after 2nd h) and 3rd i) iteration process respectively.

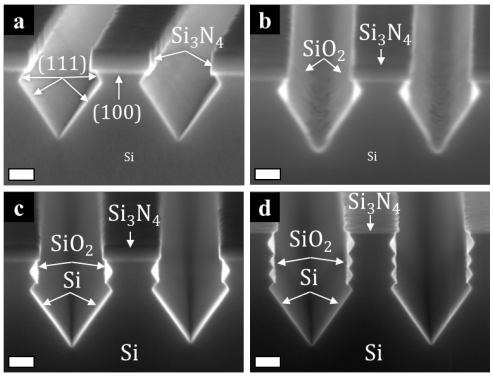

Figure 2: SEM images of fabricated vertically stacked 3D nanostructures after (a – c) single iteration, and after (d) three iterations. The scale bars are 100 nm.

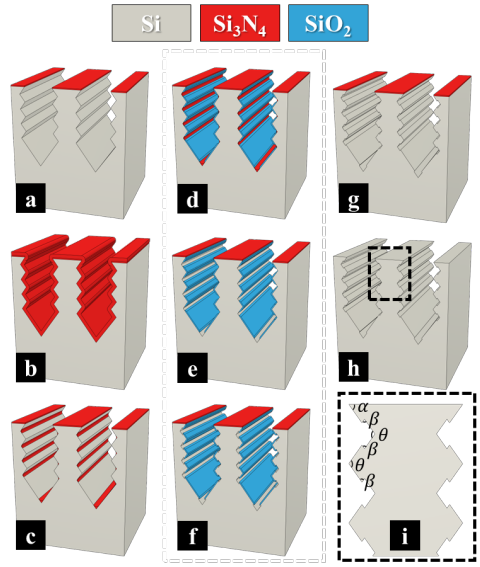

Figure 3: Schematic process flow of the sidewall patterning of vertically stacked 3D nanostructures using concave corner lithography. Starting from the 3rd iteration a), a conformal deposited layer of LPCVD Si_3N_4 b) is timed etched in H_3PO_4 c). Local oxidation of silicon (LOCOS) d) is followed by stripping the remaining Si_3N_4 in H_3PO_4 e) and finally KOH etching of concave corners f). HF etching is used to selectively strip the SiO_2 g) and the Si_3N_4 h). Cross-sectional view i) of the dashed black box in h). The sidewall structures are bounded by (111) surface creating angles α, β, θ are 54.7°, 109.4°, and 70.6°, respectively.

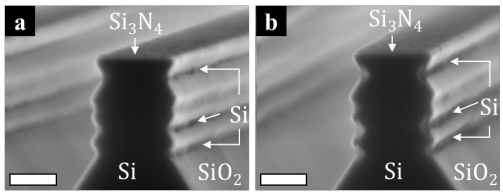

Figure 4: SEM images of side-wall patterned nanostructures after corner lithography and KOH etching of the concave corners (a) and prolonged etching (b) to make it accessible for further processing. The scale bars are 100 nm.