Engineered strain in 2D semiconductor during the growth on grayscale nanopatterned surfaces

B. Erbas[a], A. Bala[b], G. Boero[a], A. Kis[b], J. Brugger[a]
[a] *Microsystems Laboratory &* [b] *Laboratory of Nanoscale Electronics and Structures, EPFL, 1015 Lausanne, Switzerland*
berke.erbas@epfl.ch

Transistors based on 2D materials, such as MoS_2, hold promise for logic device scaling due to their sub-nanometer thickness and energy efficiency with low off-currents. However, they have electron mobilities of 20 to 30 $cm^2/V{\cdot}s$ that fall short of the *International Roadmap for Devices and Systems* projected requirements, 100 $cm^2/V{\cdot}s$ for *2nm node* GAAFETs[1]. Strain engineering, successfully applied in commercial Si MOSFETs, is a candidate for enhancing electron mobilities in MoS_2. Promising results including silicon nitride capping[2] and strain via pre-structured substrates[3] were introduced. We recently demonstrated up to an 8-fold mobility enhancement in monolayer MoS_2 FETs with 1% tensile strain through the mechanical elongation of the 2D layer during an imprinting process.[4] All presented approaches where strain is induced on pre-structured surfaces rely on polymer-assisted material transfer from a growth substrate to target surfaces. Such approach faces challenges in nanoelectronics compatibility and scalability, as defects and contamination limit its potential for high-yield production.

As a remedy, we present a new approach in which strain in MoS_2 is introduced *during* its growth process using a grayscale-patterned thin film (patent-pending), instead of a flat substrate. During the cooling phase, the respective surface length change for flat and grayscale (sine-shaped) segments differ due to thermal expansion mismatch between the Si or sapphire substrate and thin film SiO_2. This results in deterministically induced strain in grown 2D materials, depending on the depth-to-pitch ratios of the patterns (Figure 1). Sine-shaped SiO_2 patterns were fabricated using grayscale nanoimprint lithography followed by pattern transfer from resist into SiO_2. The surface roughness was controlled through thermal annealing steps and gentle plasma etching.[5] Grayscale stamps used for this nanopattern replication were made by thermal scanning probe lithography and dry etching. The CVD-grown MoS_2 on the sine-shape surface resulted in up to 0.8% tensile strain, which is known to improve FET mobilities[4] to >100 $cm^2/V{\cdot}s$, confirmed by the 40 meV photoluminescence (PL) peak shift (Figure 2). The presented approach that combines grayscale lithography and transfer-free strained growth of 2D materials is CMOS-compatible, scalable, and allows for reproducible fabrication of strain-engineered high-mobility FET channels.

1. IEEE International Roadmap for Devices and Systems (IRDS), *IRDS™ 2023: More Moore*, p. 12. Available: https://irds.ieee.org/
2. Jaikissoon, M. *et al.* CMOS-compatible strain engineering for monolayer semiconductor transistors. *Nat. Electron.* **7**, 885–891 (2024).
3. Liu, T. *et al.* Crested two-dimensional transistors. *Nat. Nanotechnol.* **14**, 223–226 (2019).
4. Liu, X. *et al.* Deterministic grayscale nanotopography to engineer mobilities in strained MoS_2 FETs. *Nat. Commun.* **15**, 6934 (2024).
5. Erbas, B. *et al.* Combining thermal scanning probe lithography and dry etching for grayscale nanopattern amplification. *Microsyst. Nanoeng.* **10**, 1–10 (2024).

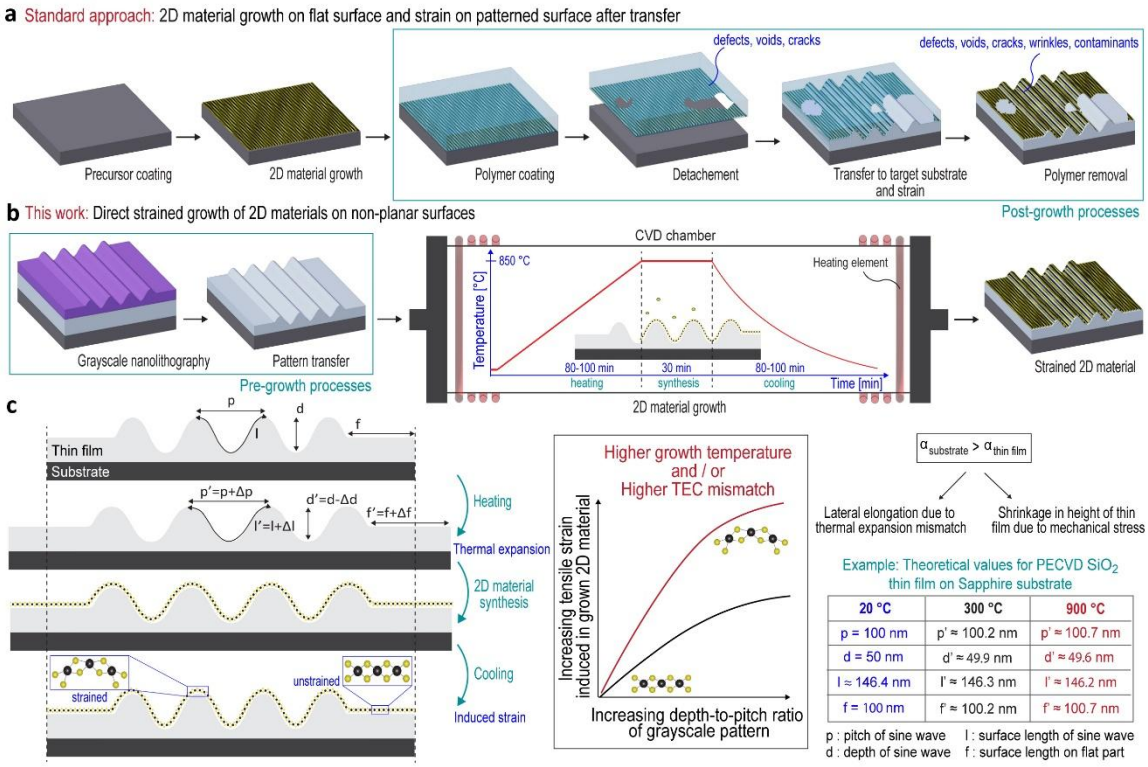

Figure 1: Schematics of (a) conventional 2D material growth and transfer for strain, and (b) strain-engineered growth on non-planar surfaces with (c) analytically calculated details.

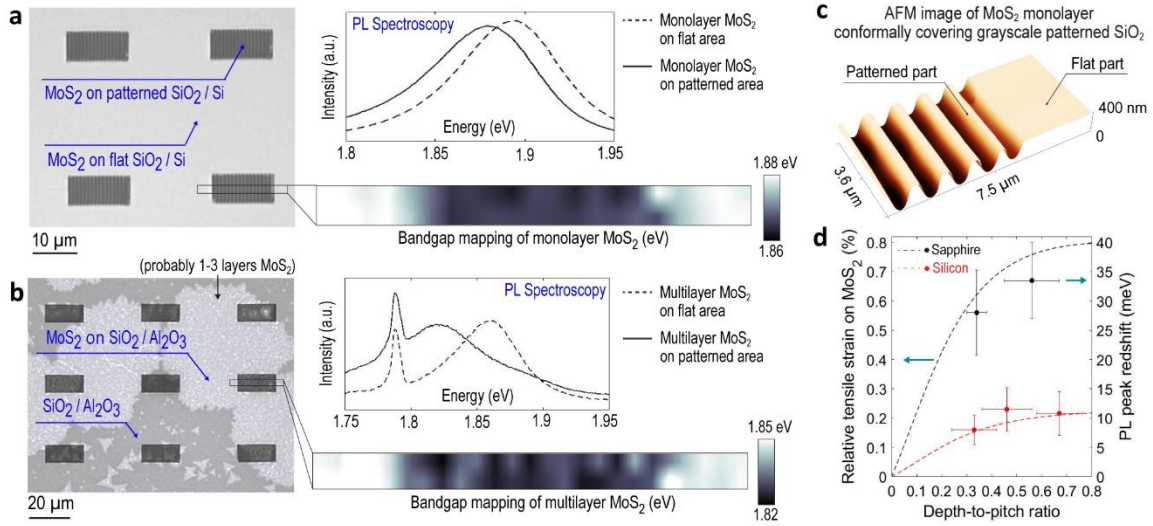

Figure 2: Photoluminescence (PL) mapping of MoS_2 grown on flat and grayscale nanopatterns fabricated on (a) thermal SiO_2 on silicon (surface fully covered) and (b) PECVD SiO_2 on sapphire (isolated triangular or merged flake). (c) AFM image, showing conformally grown MoS_2 on the pre-patterned substrate from (a). (d) Calculated strain values vs depth-to-pitch ratio (dashed line) and measured PL energy peak shifts vs depth-to-pitch ratio.