Gate width variation for MOS quantum dot formation

J.M. Pomeroy[1], P.N. Namboodiri, M.D. Stewart, Jr., Y. Hong, Z.H. Levine
Physical Measurements Laboratory, National Institute of Standards and Technology, 100 Bureau Dr., Gaithersburg, MD 20899

In this work, we lithographically vary a continuous, metal gate's width in a planar metal-oxide-semiconductor (MOS) quantum device to seek the formation of a single-electron-transistor (SET) using one gate voltage. This work leverages (a) narrow channel effects, i.e., the increase in threshold voltage when gate width is less than the depletion width, and (b) the divergence of the gate capacitance from a 2D form when the gate width is less than ≈100 nm. Our approach is to fabricate a series of "nano-wire" transistors and "bubble-gate" transistors, like the one shown in Figure 1, to find a pattern of channel, neck, and bubble widths where a single applied voltage can achieve an electron density profile like that shown in the lower part of the figure. Improved understanding of the gate width dependence can provide better sculpting and control of the electrostatic potential in MOS quantum devices with fewer individual gates.

For the "nano-wire" transistors, a series of transistors with composite inversion gate structures are made, where photolithographically (PL) defined Ti/Pd is used to control the electron density from the overlay with the phosphorus implanted n++ ohmic regions to either side of a 20 μm gap. Within the gap in the PL, electron beam lithography is used to write a series of 25 nm thick Al wires with widths ranging from 30 nm to 1000 nm. The threshold voltages measured from the nano-wire devices will be compared with estimates from COMSOL modelling to develop a design benchmark for understanding the performance of gates with more complex width variation.

To expedite device development, we also fabricated a series of "bubble-gate" transistors in the same run with some best guess values and splits for the neck and bubble dimensions. For the case shown in Figure 1, the neck regions are 50 nm wide, the "bubble" portion for the island is 300 nm in diameter, and the auxiliary gate widths are 30 nm. Additionally, we used similar best guess values to design and fabricate double-quantum dot plus charge sensor devices (2 independent channels) with 12 gates and 4 ohmics that could be used for qubit formation, but put extra pressure on the lithographic performance, and may reveal consequences from cross-capacitances. We expect to present experimental and modelling results evaluating this approach to SET formation for various design splits, discuss the trends observed and relationship to modelling results.

[1] Contact: *joshua.pomeroy@nist.gov*

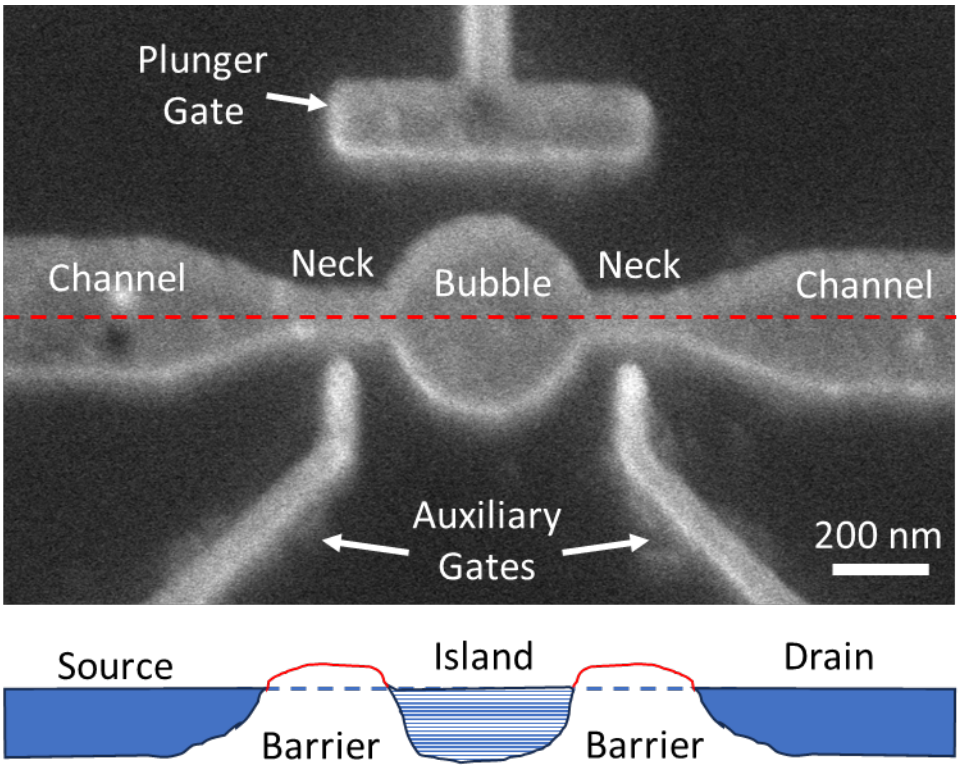

Figure 1: Scanning electron micrograph (SEM) image of a prototype "bubble-gate" transistor formed with 25 nm thick gates of aluminum on thermally oxidized, high resistivity silicon. The largest gate (aligned horizontally) inverts the silicon beneath it, forming an electron gas. Since narrow gate regions require higher voltages to invert than wide regions, we seek a voltage at which the wider source, island and drain regions are above threshold, but the narrower "necks" are below threshold, such that an electron density like that imagined in the lower cartoon can be achieved. The upper plunger can be used to tune the electron occupation on the island, while the lower auxiliary gates can be used to tweak the barriers for sharper, narrower potential profiles.