Investigation of Gate-Induced Leakage Current in Gate-All-Around Nanosheet Field-Effect Transistors

C. Cariker, D. Mamaluy, J. P. Mendez Granado, N. Modine, R. Arghavani, M. Titze
Sandia National Laboratories, New Mexico, USA
cbcarik@sandia.gov

Gate-induced drain leakage (GIDL) is a critical phenomenon that significantly impacts the performance of modern field-effect transistors, particularly as device sizes continue to scale down. Understanding the mechanisms behind GIDL is essential for optimizing device performance and reliability. In this study, we investigate the sources of GIDL in gate-all-around field-effect transistors (GAAFETs) and demonstrate that it is not a result of band-to-band tunneling (BTBT), but rather a new effect related to direct tunneling from the gate to the drain through the high-k dielectric.

The unique geometry of GAAFETs provides complete isolation of the channel from the substrate, effectively preventing BTBT from occurring between the substrate and the drain. This structural feature minimizes the electric field strength in the channel region, making BTBT from the channel to the drain unlikely. Instead, our findings reveal that GIDL arises primarily from direct gate tunneling (GDT), which occurs as carriers tunnel from the gate to the drain through the high-k dielectric layer.

To explore these effects, we measured the gate, source, and drain currents as a function of gate voltage across various device temperatures. The increasing drain current at progressively larger negative gate biases, as shown in the I-V measurements in Figure 1, indicates the presence of GIDL, which is observed to be temperature-dependent, increasing as the device warms. Figure 2 illustrates that at gate biases lower than those required to initiate source-drain current, the currents measured on the gate and drain are nearly identical in magnitude and opposite in sign, while the drain current remains flat and near-zero. This observation further supports the conclusion that GDT, rather than BTBT or direct tunneling between the source and drain, is the dominant contributor to GIDL in GAAFETs. Fully quantum mechanical 2D simulations of the device under various bias conditions and temperatures corroborate the experimental results, revealing drain-induced barrier lowering between the gate and drain as the underlying cause of the observed GDT current.

This work provides valuable insights into the mechanisms governing GIDL in GAAFETs, highlighting the novel role of direct gate tunneling in influencing device performance.

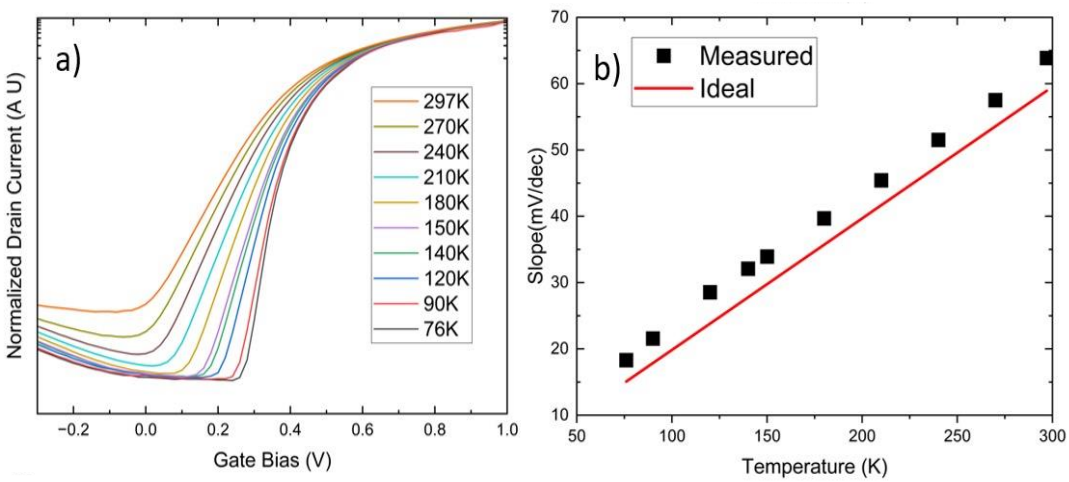

Figure 1: a) Drain current versus gate bias in a GAAFET device measured from 76 K to 297 K. In the subthreshold regime GIDL is observed as the leakage current increases at progressively larger negative gate bias. b) Slope of the IV curves measured in a) at the threshold voltage (black squares), compared to the theoretical ideal slope (red line).

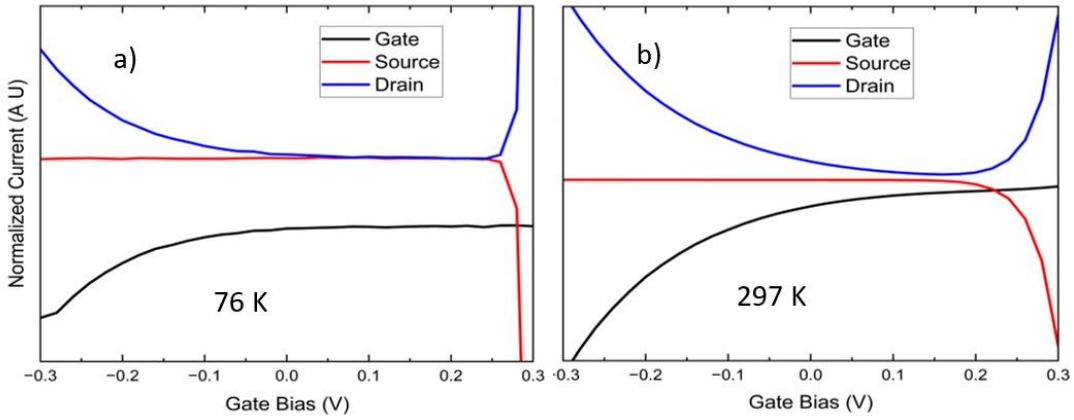

Figure 2: Normalized subthreshold leakage current flowing through the gate, source, and drain at a) 76 K and b) 297 K. In both cases, gate-drain tunneling is responsible for the observed GIDL.