Atom Defined Wires for Atomic Silicon Electronics

Abstract

The continued development and scaling down of conventional complementary metal-oxide semiconductor devices is approaching fundamental limits related to power density scaling and heat generation.[1] As a result, innovative circuit designs built from the ground up with individual dangling bonds (DBs) are in development to overcome many of these limitations, offering significant improvements in miniaturization and efficiency.[2]

Using the ultra-sharp tip of a scanning tunneling microscope (STM), individual H-Si bonds can be broken, as pioneered by Lyding et al.,[3] to create DB circuitry on the H-Si (100) surface. Advances in error correction and precision now allows for the fabrication of error free atomic structures and has opened the door to a variety of applications.[4] By manipulating electrons in DB structures, different binary logic operations can be performed.[2] The function and design of these DB circuits (Figure 1) is explained along with software tools which are used for modeling and simulation.[5]

In this presentation we also explore DB wires which are crucial for transmitting signals across the Si surface and biasing other circuit elements. Several different error free DB wires were characterized at 4.5 K under near identical conditions to determine the optimal DB wire geometry. dI/dV line spectroscopies (Figure 2) over each wire reveal their local density of states and show how small changes in DB geometry impact bonding interactions and cause new states to emerge. DFT modelling and transmission calculations were also done to determine which wire geometries have the most favourable transport characteristics. The effects of hydrogen defects, as well as nearby charge centers are discussed. Finally, the screening properties of a DB box are illustrated. Through these efforts we have made some steps toward the goal of establishing fabrication and characterization techniques for next generation devices.

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3. Lyding, J. W., Shen, T.-C., Hubacek, J. S., Tucker, J. R. & Abeln, G. C. Nanoscale patterning and oxidation of H-passivated Si(100)-2×1 surfaces with an ultrahigh vacuum scanning tunneling microscope. *Appl. Phys. Lett.* **64**, 2010–2012 (1994).
4. Pitters, J. *et al.* Atomically Precise Manufacturing of Silicon Electronics. *ACS Nano* **18**, 6766–6816 (2024).
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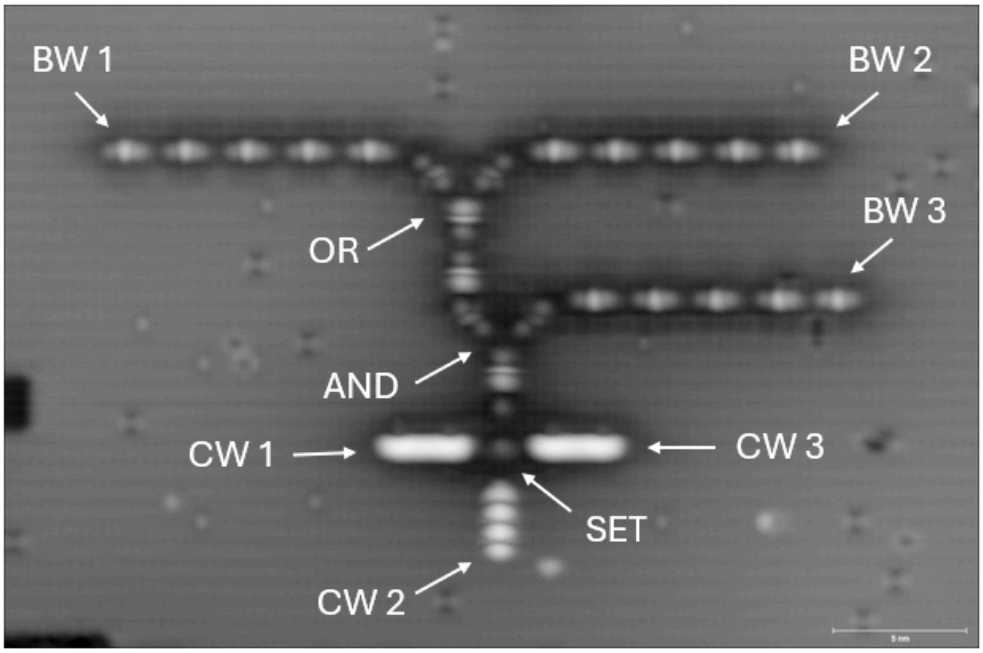

Figure 1. A first prototype atomic silicon integrated circuit is shown. 1.3 V, 50 pA STM image of a three input combination OR gate and AND gate with an atom-defined SET readout formed out of 69 DBs. The circuit was designed using DB modelling and simulation software (SiQAD).

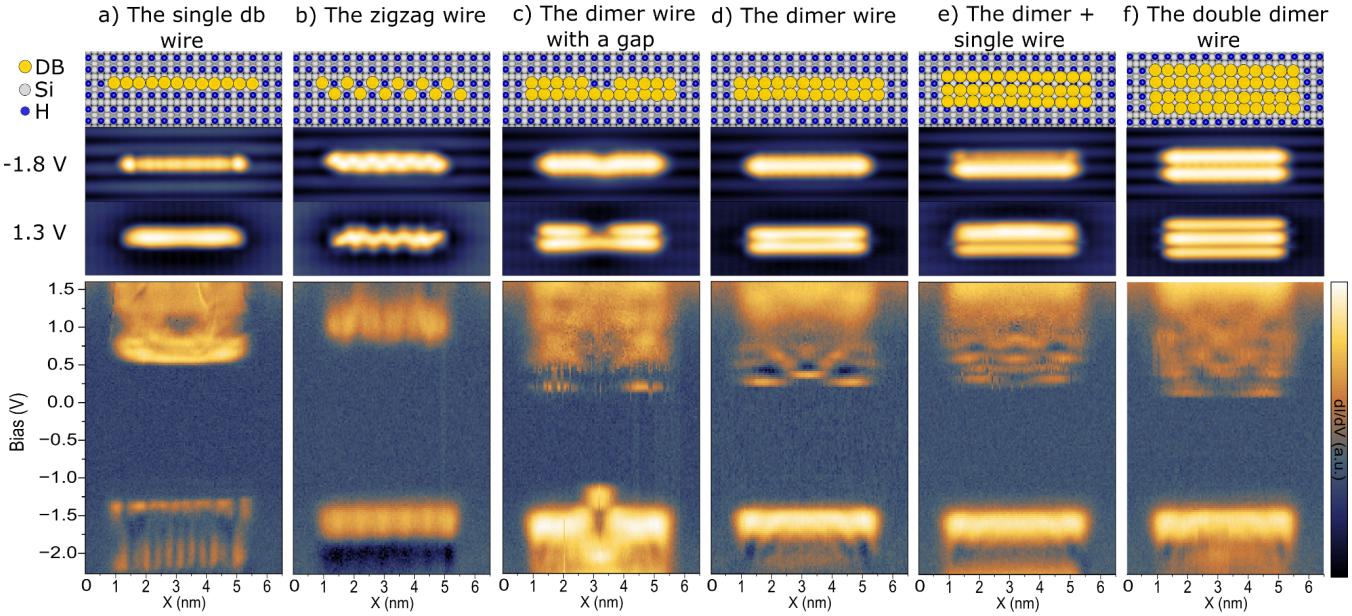

Figure 2. Ball and stick models, STM images (50pA), and dI/dV maps for the sequence of six dangling bond wires that were sequentially fabricated. Measuring the wires in the same crystal location and with consistent tip conditions allows for the LDOS of each wire to be directly comparable. The dimerized wires show quantum in-gap states that are calculated to have favourable transport characteristics.