Fabrication of Atomically-precise Nanoimprint Masks by STM Lithography

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The Semiconductor industry, is struggling to continue to follow Moore's Law. For both technical and economic reasons, it is likely that the current ASML EUV tools will be the last photolithography technology to push to higher resolutions. Simultaneously, E-Beam Lithography mask writers, while improving throughput by going highly parallel, are also very near the end of resolution improvements. The industry does not appear to expect any significant downscaling of devices beyond what will be possible with the ASML High-NA EUV tool which has a resolution of 8 nm. Furthermore, the DOE Advanced Materials and Manufacturing Technologies Office (AMMTO) sponsored Semiconductor Industry Energy Efficiency Scaling (EES2) roadmap has identified Extreme Ultraviolet Lithography (EUV) as a significant contributor to the energy budget of advanced digital electronics. Strikingly, EUV is so inefficient that only about 0.04% of the beam energy actually affects the resist.

The EES2 roadmap identifies the replacement of EUV with Nanoimprint lithography (NIL) as a key takeaway. NIL offers equal and better resolution and precision than EUV, with up to 90% lower energy costs, resulting in lower costs of production. However, NIL uses a mold of the pattern to be printed on the wafer as a mask and the best resolution of the current mask writers, using E-Beam lithography (EBL), is 15nm. This means that it is critical to adopt a mask writing technology with better resolution than EBL, otherwise the industry will be much less likely to adopt NIL as a preferred lithography technology. It must provide resolution at least as good as the High NA EUV tool's 8nm to be widely adopted.

This presentation will describe a pathway towards unprecedented resolution in nanoimprint mask fabrication. Ultrahigh-precision NIL templates are made by writing sub-nm precision patterns on Si(001) using H Depassivation Lithography (HDL), followed by selective growth via atomic layer deposition (ALD) of a hard mask such as TiO_2, which is then used as an etch mask for Reactive Ion Etching (RIE) to form a Si template, replicating the STM pattern. This template would then be transferred into a quartz template using existing step and flash NIL processes which will be used to pattern devices on the die or wafer scale. We show that sub-10 nm feature sizes and full-pitch gratings with feature radius of curvature down to 1.5 nm in the lateral dimension are achievable. This process therefore addresses the EES2 goal of improving the energy efficiency during manufacturing of digital electronics.

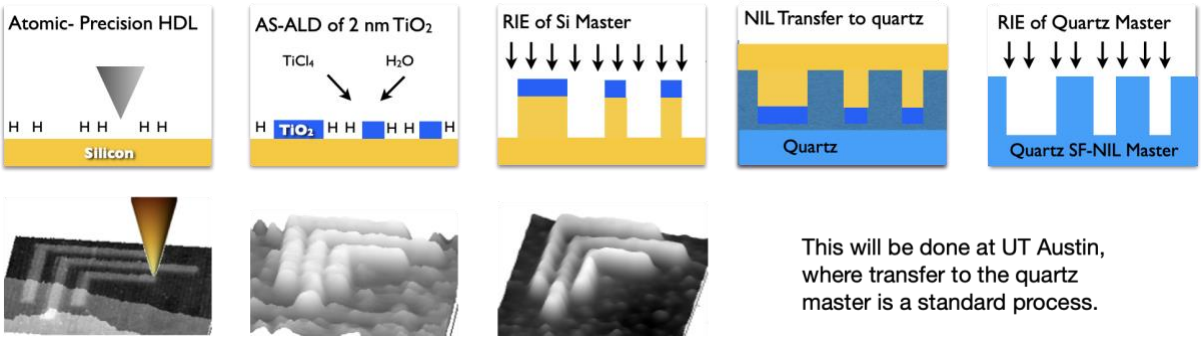

Fig. 1: (From left): Sub-nm precision patterns written using H Depassivation Lithography on Si(001):H. Atomic Layer Deposition of TiO_2 etch mask. Reactive Ion Etching with to make a Si master. The next step is to use Nanoimprint Lithography and RIE to produce a quartz master.

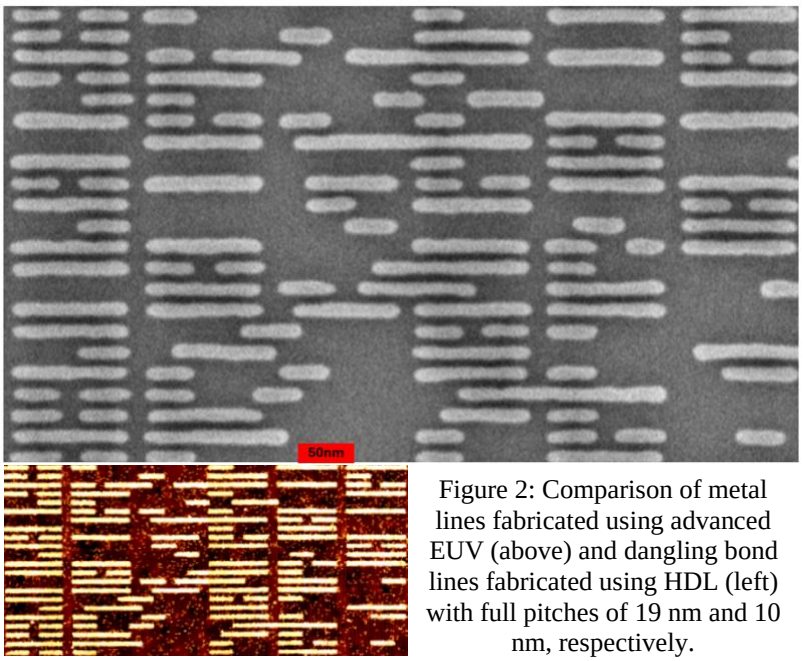

Figure 2: Comparison of metal lines fabricated using advanced EUV (above) and dangling bond lines fabricated using HDL (left) with full pitches of 19 nm and 10 nm, respectively.