EUV lithography: history, latest results, what's next

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Abstract:

Research on EUV lithography started in the mid-1980s. The long history of its development will be briefly reviewed by someone who was a rather late participant in this process. EUV lithography entered the high-volume production of semiconductor chips in 2019, at the 7-nm node of logic integrated circuits, and enabled the continuation of Moore's Law. Since then, the technology has been used in the production and research and development of advanced logic and DRAM chips, and the performance of EUV exposure systems continues to improve. 0.55 NA exposure systems became available in 2024 and lithographic results from such a system will be shown. This high-numerical-aperture EUV lithography will enable continued scaling of logic and DRAM devices, and perhaps new-type devices of the future. The presentation will conclude with a discussion on resolution and process window enhancement and ASML's EUV technology roadmap.