Accelerating Multiple Patterning Decomposition with an Analog 3-SAT Solver

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Multiple patterning is a crucial technique in advanced nanofabrication to overcome the limitations of optical lithography. As feature sizes shrink and design complexity increases, solving the decomposition problem efficiently becomes a significant challenge. Graph coloring is a well-established approach for addressing this problem, where layout geometries are mapped to a graph and assigned colors representing different patterning masks[1]. However, conventional computational methods for solving large-scale graph coloring problems often suffer from high computational costs, making them impractical for complex layouts.

In this work, we propose an analog 3-SAT accelerator[2] to solve the multiple patterning decomposition problem efficiently. We first model the decomposition problem as a graph coloring problem and then convert it into a 3-SAT formulation. Our accelerator, designed with circuit feedback mechanisms, naturally settles into a stable state representing a valid solution. By leveraging the parallelism and continuous-time dynamics of analog computation, our approach achieves a significant speed advantage over traditional digital solvers. Unlike conventional logic-based methods that rely on extensive search operations, our system explores solution spaces efficiently through analog behavior, leading to rapid convergence even for complex cases. Its ability to adapt dynamically to variations in problem constraints makes it a promising solution for real-world lithographic challenges.

Figure 1 illustrates the flow of layout decomposition for multiple patterning. The process begins with an algorithm that detects spacing violations and transforms the input pattern into a graph coloring problem. This graph coloring problem is then converted into an SAT problem. Figure 2 provides a detailed mapping of the graph coloring problem to a 3-SAT formulation, which serves as the input for our analog 3-SAT solver. Figure 3 presents the circuit of the analog 3-SAT solver and its corresponding variable assignment output. The reconstructed pattern decomposition confirms the effectiveness and feasibility of this approach.

1. I. H. -R. Jiang and H. -Y. Chang, "Multiple Patterning Layout Decomposition Considering Complex Coloring Rules and Density Balancing," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 36, no. 12, pp. 2080-2092, Dec. 2017, doi: 10.1109/TCAD.2017.2681068.
2. Q. Zhang*, S. Su*, Z. Liu*, H.-C. Cheng, Z. Qiu, M. Palaria, J. Ye, D. Meng, B. Chen, S. Hossain, W. Wu, M. S.-W. Chen, "A Stochastic Analog SAT Solver in 65nm CMOS Achieving 6.6μs Average Solution Time with 100% Solvability for Hard 3-SAT Problems," in *IEEE Symposium on VLSI Technology and Circuits (VLSI Technol. Circuits)*, June 2024.

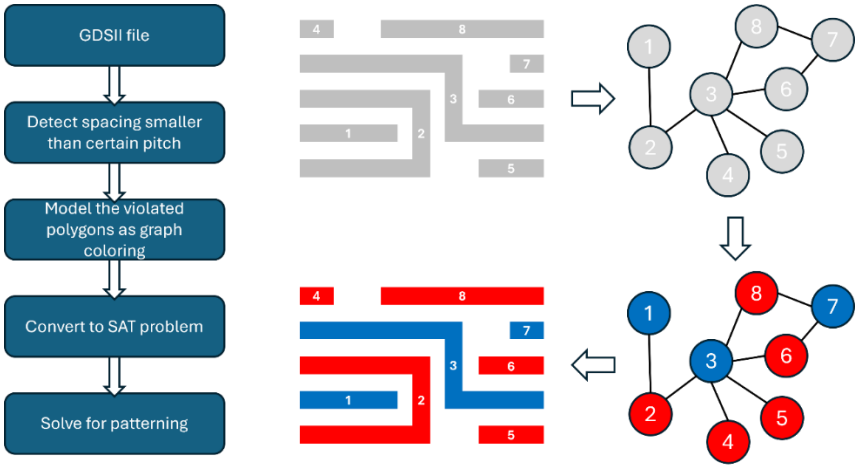

Figure 1: Layout decomposition flow for multiple patterning.

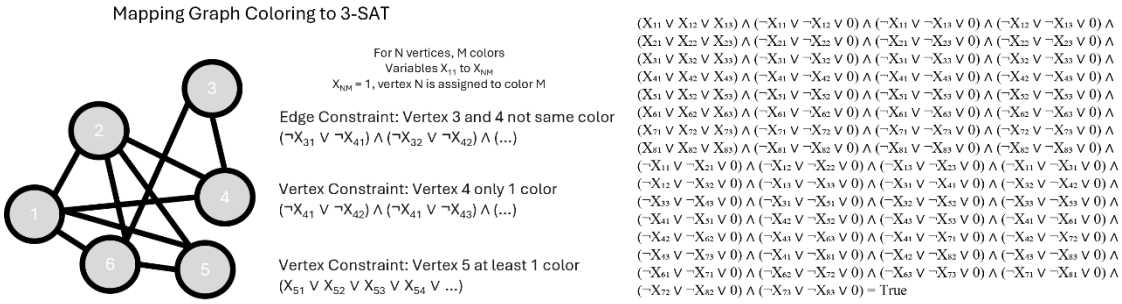

Figure 2: Mapping the graph coloring problem to an SAT formulation and the resulting CNF.

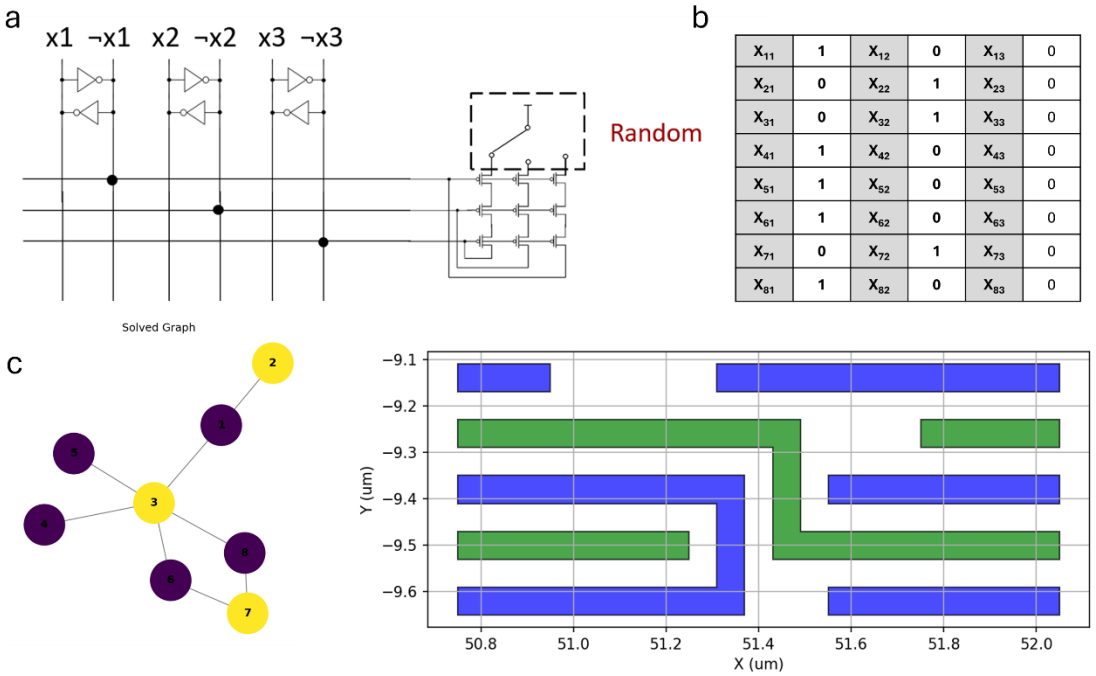

Figure 3: (a) Circuit design of the analog 3-SAT solver. (b) The variable assignment output and (c) the reconstructed pattern decomposition demonstrate the feasibility of this approach.