Abstract for
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Title: Neuromorphic Systems and the Return on Analog

The human brain has 86 billion neurons and uses approximately 20 watts of power. Computational energy efficiency is about 230 pW/neuron or 100 teraflops/W. A fly brain contains 140 thousand neurons and only uses microwatts of power. Computational energy efficiency is about 20 pW/neuron of 0.1 teraflop/W. The vast computation power and high energy efficiency comes from immense parallelism, low frequency (< 100 Hz), and low voltage pulsed analog signals.

During the 1970's there was significant research focused on analog signal processing using charge-coupled devices. As integrated circuits become more powerful, digital displaced analog in the 1980's because digital offered simpler designs, and "higher" accuracy. In the early 2000's CPU clock speeds started to stagnate. The balance between power required and heat generated had reached the practical limit. "Intel reports that underclocking a single core by 20 percent saves half the power while sacrificing just 13 percent of the performance." [1].

Digital computer architectures are now focusing on compute-in-memory. Compute-in-memory for analog signal processing goes back to before 1970 [2]. Analog technology is already fully parallel from biological systems to analog signal processing. Analog multipliers only require 17% of the transistor count compared to a digital multiplier [3]. Analog multipliers are limited to around < 8 bits of resolution; however, neural networks can operate with single bit resolution. Recent developments in memristor, stored charge field effect transistors, ferroelectric memories offer high density analog memories for analog computation.

What is missing are design rules for ~10 nm analog libraries. IC fabrication industry and IC software design tool developers need to address analog devices for low power neuromorphic applications. Biological brains are not "clocked" like conventional digital. Biological brains operate more of in a handshake asynchronous mode. IC fabrication industry and IC software design tool developers also need to consider asynchronous [4], event driven [5], and continuous time systems [6] to take advantage of the low power sensing and signal processing methods. A third area are design tools for analog sense-compute-in-memory architectures [7].

[1] https://spectrum.ieee.org/why-cpu-frequency-stalled

[2] A. Noda, "Leak-compensated analog memory with pair mosfets," in *IEEE Journal of Solid-State Circuits*, vol. 5, no. 2, pp. 75-77, April 1970, doi: 10.1109/JSSC.1970.1050075.

[3] S. Mullapudi, "Current-Mode Analog Multiplier Based on Translinear Loops" in , State University of New York at Buffalo, Master of Science in Engineering, August 2018.

[4] K. Y. Yun: "Recent advances in asynchronous design methodologies," *Proceedings of the ASP-DAC '99 Asia and South Pacific Design Automation Conference 1999 (Cat. No.99EX198)*, vol.1, pp. 253-259, Hong Kong, China, 1999. doi: 10.1109/ASPDAC.1999.760008.

[5] A. Rahmatulloh, et al.: "Event-Driven Architecture to Improve Performance and Scalability in Microservices-Based Systems," *2022 International Conference Advancement in Data Science, E-learning and Information Systems,* pp. 01-06, Bandung, Indonesia, 2022. doi: 10.1109/ICADEIS56544.2022.10037390.

[6] Y. Tsividis, "Event-Driven Data Acquisition and Digital Signal Processing-A Tutorial", *IEEE Transactions on Circuits and Systems-II: Express Briefs*, vol. 57, no. 8, 2010.

[7] D. Reis, et al.: "Computing in memory with FeFETs," Proceedings of the International Symposium on Low Power Electronics and Design, Association for Computing Machinery, Article 24, pp. 1–6. New York, NY, USA. https://doi.org/10.1145/3218603.3218640.