Research to Manufacturing: Developments in Displacement Talbot Lithography (DTL) for Semiconductor Lasers

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The rapid expansion of artificial intelligence, driven by large-language models and data-intensive computing, is accelerating research and demand for high-performance semiconductor lasers such as vertical-cavity surface-emitting lasers (VCSELs), distributed feedback (DFB) lasers, and other related devices. These products are critical not only for data centers, but also LIDARs, sensing, and other longer range optical communications. Their performance relies on high-resolution periodic nanostructures that enable single-mode operation, beam shaping, polarization control, and wavelength stability. As research efforts increase and production volume grows, both R&D and manufacturing require lithography solutions that combine resolution, throughput, and cost efficiency. Recent developments make DTL the ideal technology for achieving this.

DTL provides several unique advantages for laser manufacturing. It supports extremely large single-exposure fields, up to 140 x 140 mm^2, with excellent pattern uniformity. Gratings can be printed at resolutions down to 62.5 nm half-pitch and remarkable pitch accuracy, which has been characterized down to the single-digit picometer range across a full wafer. Such accuracy is critical for wavelength selective devices. DTL's large depth of focus and non-contact exposure make it suitable for variable surface topography and diverse substrates, including InP, GaAs, GaN, SiC, Si, and glass.

Modern VCSEL designs often incorporate high-resolution surface gratings for polarization control, beam shaping, and as high-reflectivity mirrors. DTL enables wafer-scale grating patterning, typically combined with a subsequent low-resolution lithography step to define laser cell boundaries as shown in Fig. 1. VCSELs fabricated using DTL have demonstrated orthogonal polarization suppression rations of up to 30 dB[1], and studies show DTL capable of replacing electron-beam lithography (EBL) for surface periodic gratings[2].

For DFB and Distributed Bragg Reflector (DBR) lasers, inclusion of a quarter-wave phase shift is needed for a stable single-mode operation. Traditionally, this phase shift is introduced abruptly by modifying a single grating period. DTL provides an equivalent solution by implementing a gradual phase shift over several grating periods, which accurately achieves the same total phase shift value. A schematic drawing of the phase profile is shown in Fig. 2(a). Preliminary results demonstrate that this approach achieves performance comparable to conventional designs. Devices fabricated with this method exhibit an average single-mode suppression ratio (SMSR) of 42.65 dB at room temperature and 42.57 dB at high temperature, as shown in Fig. 2(b), with a high yield for a grating pitch of approximately 203 nm. With further iteration and optimization of the phase shift design and the following process control, a higher SMSR is expected.

Beyond one-dimensional gratings, DTL is capable of patterning the two-dimensional periodic arrays required for photonic crystal surface-emitting lasers (PCSELs). Recent advances in DTL's two-dimensional capabilities have been enabled by inverse mask design (IMD) techniques[3].

In conclusion, recent developments with Displacement Talbot Lithography, including gradual phase shift implementations and two-dimensional array patterning, have expanded opportunities across laser research, development, and manufacturing.

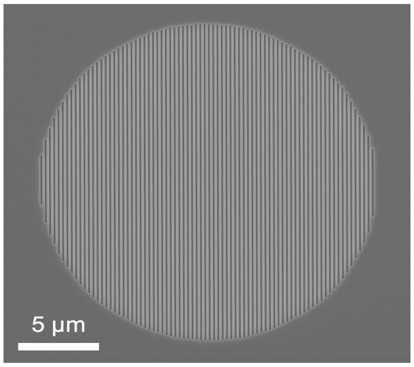

Fig. 1. SEM image representing a typical VCSEL cell with surface gratings. The high-resolution grating (280 nm pitch) is patterned with DTL and the 22 µm circular boundary was sharply defined in a subsequent low-resolution lithography step.

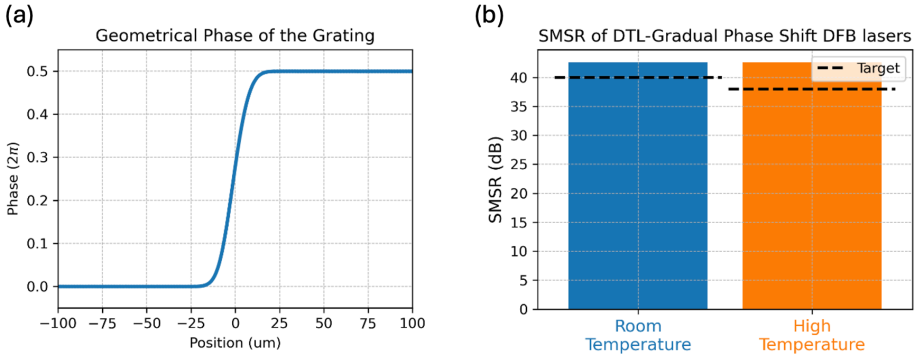

Fig. 2. (a) The phase profile of a gradual phase shift design compatible with DTL exposure. The total phase shift is precisely defined as π, which inverts the relative location of the grating lines. (b) Experimentally measured Single-Mode Suppression Ratio (SMSR) for DFB lasers patterned with DTL, incorporating the gradual phase shift design. The SMSR values exceed the device target at both room and high temperatures.

References

1) Yingying Liu, et al., *Appl. Opt.* **57**, 4486 (2018
2) Zhu Shi, et al., *Proc. SPIE* **12556** (2023)Zhu Shi, et al., *Proc. SPIE* **12556** (2023)
3) (Rietmann et al., *Proc. SPIE* **13424**, 134240G (2025)

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