DRIE Defects and Mitigation with Plasma Smoothing for Superconducting Through-Silicon Vias

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Superconducting through-silicon vias (ScTSVs) are receiving increasing interest for interconnects and isolation in superconducting quantum information systems[1]. Crucially, via processes must integrate with existing planar superconducting fabrication processes and provide a smooth sidewall surface for subsequent superconductor deposition. Previously reported processes and our metallization attempts highlight the difficulty of creating such a smooth sidewall[2]. The proposed via-first fabrication process (figure 1) involves deposition and patterning of a SiO_2 hard mask for deep reactive ion etching (DRIE) and wafer thinning to expose vias. We identify DRIE defects, including an underreported 'blowout' defect that emerges when active etch area is <1%, and we present a smoothing etch chemistry comparison showing CF_4/O_2 provides the greatest improvement in surface morphology and a wide process window for ScTSV integration.

Cross-sectional SEM reveals three dominant DRIE defect types (Figure 2). Firstly, scalloping, which is inherent to the cyclical Bosch-type process commonly used for Si DRIE. Secondly, vertical mask erosion defects which are consistent with hard mask edge erosion during the etch. Lastly, we observe deep sidewall gouging or blowout, which has not been widely reported. Sidewall blowout becomes significant when the fraction of exposed silicon on a particular etch pattern is extremely low, as shown in figure 3. When a SiO_2 hard mask with full edge coverage is used with a sparse pattern, the active etch area can be less than 0.015% of the wafer area. We hypothesize that this causes an extremely high etch rate by a comparable mechanism to the well-studied etch rate decrease from plasma loading. To mitigate this issue, we implement sacrificial etch regions on low density patterns to increase active etch area.

We analyze and compare smoothing etches with SF_6/Ar, SF_6/O_2, and CF_4/O_2 chemistries in an inductively coupled plasma etcher with parameters similar to previously published work (figure 4). SF_6/Ar etches show a high etch rate of approximately 10 um/min, but surface morphology is worsened. A SF_6/O_2 etch shows a lower etch rate of ~0.5 um/min and a significantly improved surface. CF_4/O_2 based etches show a low rate around 60 nm/min and an excellent resultant surface morphology. Further, the studied CF_4/O_2 etch preserves polished Si roughness (Ra) below 2 nm, allowing long etches to be used without concern for SiO_2 selectivity. With a wide process window and excellent smoothing characteristics, this CF_4/O_2 etch is an ideal tool for TSV sidewall smoothing.

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[1] J. A. Alfaro-Barrantes *et al.*, IEEE Electron Device Letters **41**, 1114 (2020).

[2] Z. Ren *et al.,* IEEE Electron Device Letters **46**, 175 (2025).

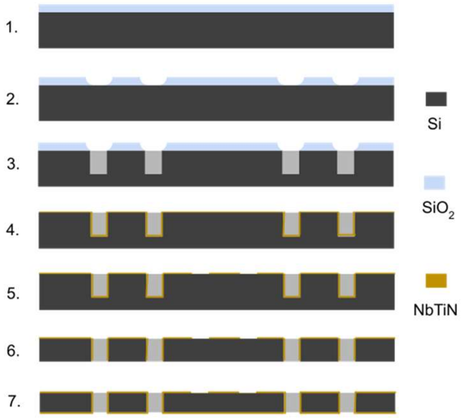

Figure 1: Proposed fabrication processes flow. 1) SiO2 hard mask deposition. 2) Hard mask patterning. 3) DRIE and post smoothing. 4) Front side metallization. 5) Front side patterning. 6) Wafer thinning. 7) Back side metallization.

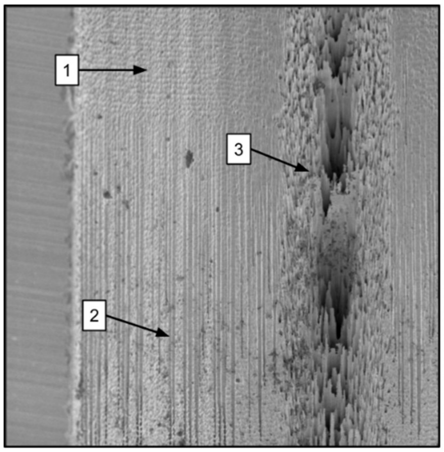

Figure 2: Select DRIE sidewall defects including 1) sidewall scalloping, 2) vertical mask erosion artifacts, and 3) sidewall blowout.

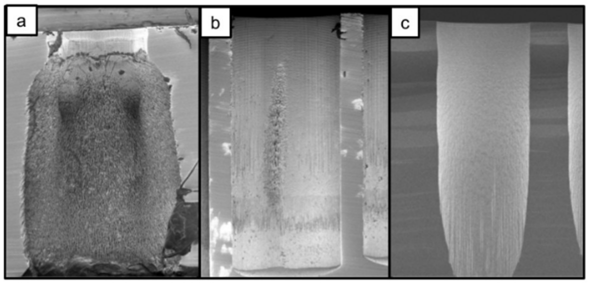

Figure 3: Via cross sections with active etch fractions of a) 0.014%, b) 0.49%, and c) >0.90% of wafer area.

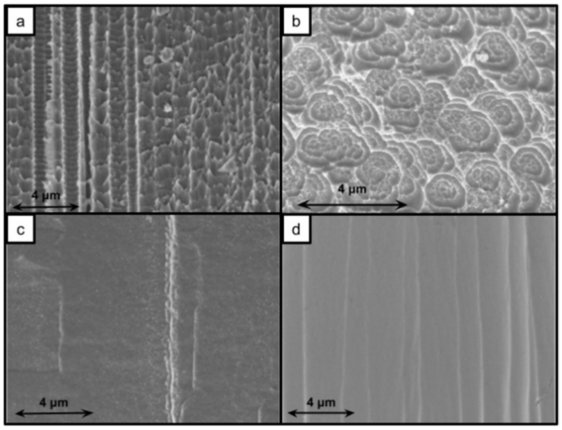

Figure 4: Via sidewall surface after various etch chemistry: a) Pre-smoothing, b) SF_6/Ar, c) SF_6/O_2, d) CF_4/O_2.

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