Optimizing Electrical Contacts to Atomically Precise Quantum Devices

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A scanning tunneling microscope (STM) can be used to fabricate devices on a hydrogen passivated silicon surface with atomic precision. Such devices provide an intuitive solid-state platform in silicon for quantum computing and simulation. Dosing phosphene or diborane onto a patterned silicon surface allows either phosphorus or boron to be incorporated where hydrogen atoms were removed. About 30 nm of epitaxial intrinsic silicon is overgrown to encapsulate the device, which allows it to be shelf-stable outside of an ultra-high vacuum environment.

Several challenges emerge when fabricating such small atomic features, mainly in electrically contacting the buried devices. Large STM-patterned leads branch out from the devices to allow a greater surface area of buried degenerately doped regions to be contacted via e-beam patterned palladium silicide contacts. Such large, patterned leads are manually time consuming to fabricate. Figure 1 shows an automation platform that has been developed to automatically fabricate STM-patterned leads, including automated STM tip quality detection, tip conditioning, lithography detection, lithography quality, and tip creep correction algorithms. Figure 2 shows an optical image of palladium silicide leads contacting a buried single electron transistor device with optically patterned gold leads and pads. The gold pads are subsequently used for wire-bonding the silicon chip to a custom printed circuit board that can be mounted in a dilution refrigerator for characterizing the atomic device.

Precise depth control of silicide formation is crucial to electrically contact the degenerately doped device layer within an intrinsic envelope without interacting with the substrate layer. We have been utilizing lightly boron-doped silicon substrates to pattern atomically precise devices; however, an accumulation of boron near the interface layer of the device is suspected to reduce achievable electrical gate ranges. One approach to mitigate this issue is depositing a thin undergrowth layer (~20 nm) of intrinsic silicon or silicon-28 above the interface prior to STM patterning. This requires precise control of palladium silicide depth. This presentation will cover experiments for optimization and characterization using FESEM to target between 30 and 50 nm deep contacts. Figure 3 shows an FESEM image of a silicon chip cross-section with a palladium silicide lead. Deposition thickness, temperature, and anneal time have been varied to study palladium silicide formation.

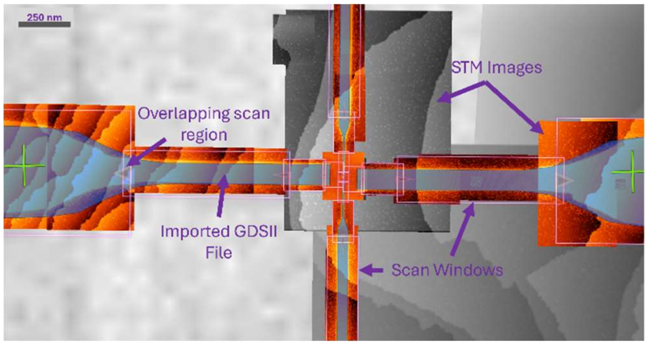

Figure 1: A screenshot of the open-source ABD Navigator STM automation software platform which enables automated feedback-controlled hydrogen de-passivation lithography. Machine learning and computer vision algorithms provide tools for automated tip quality detection and conditioning, as well as tip creep correction and lithography analysis.

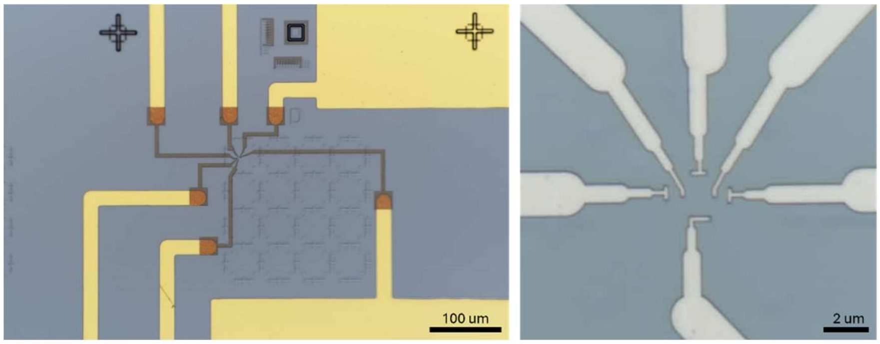

Figure 2: Optical image showing the two-step deposition process consisting of e-beam patterned palladium silicide leads (right) that contact the buried STM-patterned devices, and gold pads (left) that are used for wire-bonding and setting up electrical contacts for measurements.

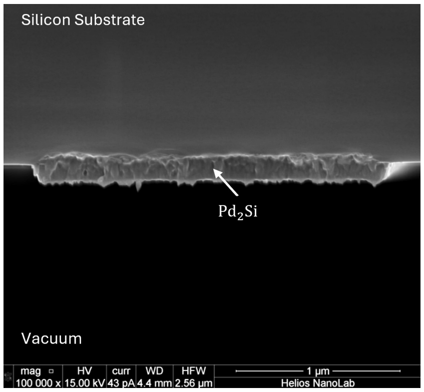

Figure 3: An FESEM image of the cross section of a silicon chip that had palladium deposited on the surface. Deposition thicknesses, annealing times, and temperatures were varied to characterize the depth of silicide formation.