Characterization of Leakage in Metallic Contact Leads for Silicon Quantum Devices

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Silicon-based dopant quantum devices have applications in quantum computing with the single electron transistor (SET) as a charge sensor and arrays of dots forming analog quantum simulators. A large gate bias window (gate range) is a requirement for effective manipulation and characterization of donor dot devices. It is essential for maximizing the number of accessible donor charge transitions observed in our single electron transistor and allowing the complete unloading of an array of dots for our analog quantum simulators. Presently, these devices are limited due to a small effective gate range of approximately ±350 mV (Figure 1).

These devices are fabricated in an ultra-high vacuum (UHV) environment on a lightly boron doped (10^{15} cm^{-3}) silicon substrate. The Si-chips are first out-gassed at 600 °C for 20 hours and then flashed five times to 1200 °C in 12-second bursts to remove the native oxide layer and other surface contaminants. Subsequently, the chips are hydrogen passivated, patterned via selective hydrogen de-passivation lithography using a scanning tunneling microscope (STM), then encapsulated in a 30 nm epitaxially grown, intrinsic layer of silicon for ambient post-processing in a cleanroom environment. Palladium is then deposited and annealed to form Pd_2Si which makes electrical contact with the buried device.

We fabricated four-lead test structures (Figure 2) on a bare, chemically cleaned silicon chip, which resulted in an effective gate range of approximately ±3 V at 4 K. However, after the standard out-gassing and flashing process, similar test structures exhibit a reduced gate range of less than ±400 mV. By sequentially varying the total flash time and the doping of the sample, we have successfully demonstrated two potential methods which significantly increase the effective gate range (Figure 3). By raising the total flash time to five minutes, we observe an increase in the effective gate range to over ±1 V. Alternatively, by using intrinsic silicon rather than lightly doped, we observe an increase in the gate range to over ±2 V. This fundamental improvement in the accessible gate space significantly enhances our ability to effectively manipulate our devices.

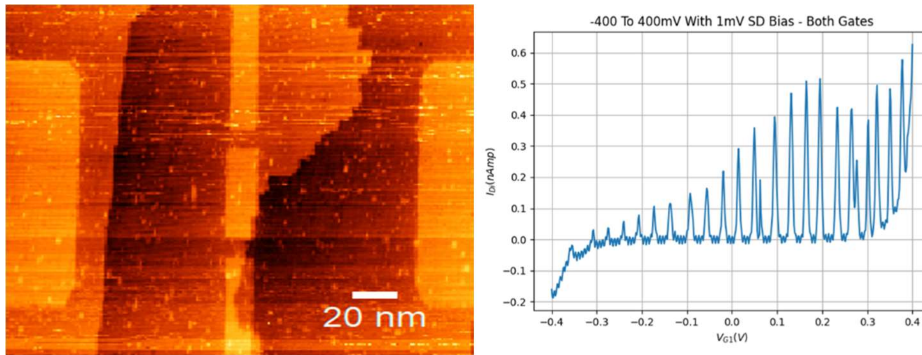

Figure 1: Image of SET and an example line sweep of the SET from -400 mV to +400 mV measured at 4 K. Beyond ±300 mV, the leakage current becomes dominant and obscures the Coulomb oscillations and charge transitions.

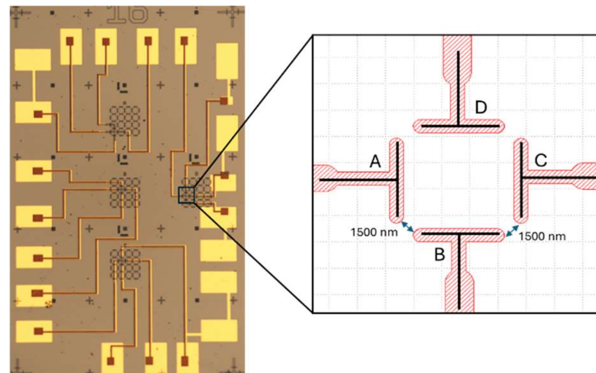

Figure 2: Example of the fabricated four lead test structure. The test structure has four different corner-to-corner spacings ranging from 600nm to 2000nm.

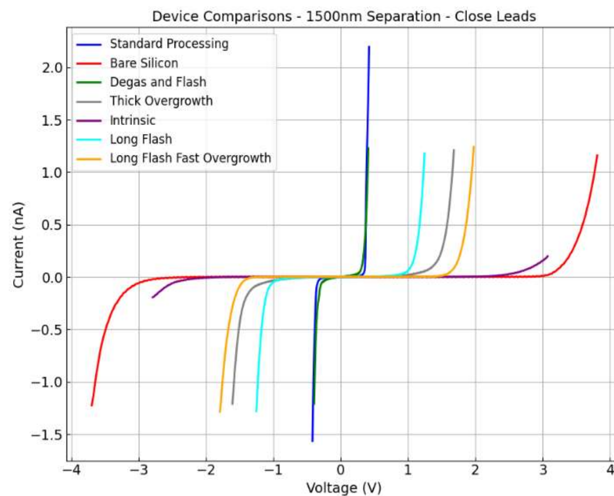

Figure 3: Summary of I-V relations for each process change measured at 4 K. We note the significant improvement over the standard processing using the long flash method and the intrinsic sample.