Bubble Gate Transistors: A single electron transistor (SET) formed using a single gate with varied widths

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A single inversion gate with non-uniform width is used to define an electron gas that has a reservoir, an isolated island, and another reservoir; thus, forming a single electron transistor, a basic building block of silicon-based quantum information. Silicon based MOS (metal-oxide-semiconductor) technology can potentially leverage the existing semiconducting manufacturing infrastructure and can further benefit from established isotopic enrichment, but faces serious challenges to scale-up in control and readout. Typical gate layouts may require 10 gates with 10 different voltages to form a single physical qubit, and novel approaches are required to reduce this physical resource load for scale-up.

Here we explore the possibility of using variation in the physical width of the inversion gate in a MOSFET geometry to form a single electron transistor. In another device type, we present a double quantum dot with an SET charge sensor. In earlier work, we found that the threshold voltage for inverting the silicon has a strong dependence on the gate width in the <200 nm regime, and here we exploit this to use a single gate to create an electron gas with a complex shape. Measurements of these “bubble gate transistors,” named due to the larger circular region of the gate where the quantum dot forms are presented: Coulomb diamonds indicating the formation of deliberate dots, and measurements of various gate capacitances that confirm dot position will be shown. Additionally, charge sensing data monitoring the double-quantum dot charge stability patterns will be presented, including the ability to modulate the coupling between the two dots, an essential element for qubit control.

While gate width variation may not ultimately be feasible in high fidelity qubit implementations, structures of this type could play an important role in process control monitoring as an extended chain of “necessary but not sufficient” metrics beyond traditional CMOS scribe line test structures. Bubble gate SET devices built in the scribe line or on sacrificial dies could provide important indicators for charge stability, threshold voltages, work functions and other material process parameters through a fabrication process flow.

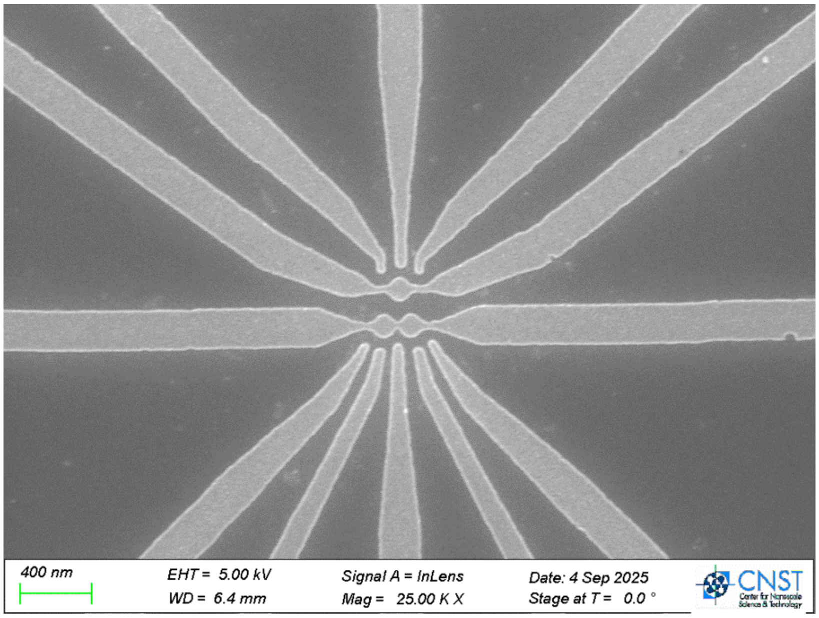

Figure 1: SEM micrograph of a device for use as a double quantum dot with charge sensor fabricated using the bubble gate transistor concept.

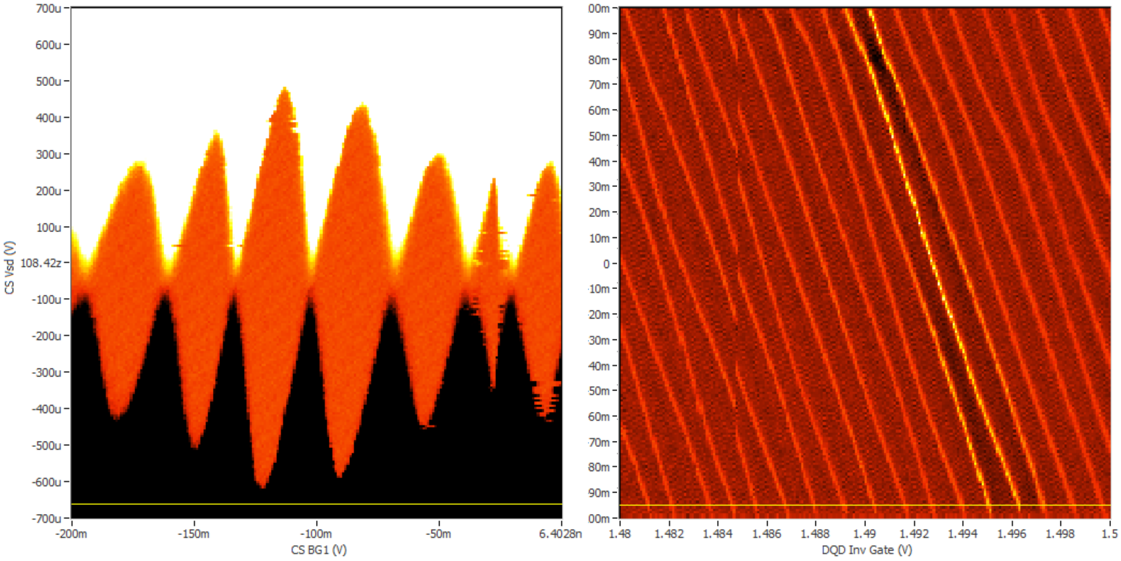

Figure 2: (left) Coulomb diamonds measured in the upper channel (charge sensor) of the device shown in Figure 1. (right) Charge sensing using the upper channel in Figure 1 as an electrometer to sense charge transitions in the lower double quantum dot, which is configured as a single large dot in this case. Measurements were conducted at <100 mK.