Correlative Laser–FIB/SEM Workflows for Metrology, Inspection, and Characterization of Advanced Microelectronics Packaging

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Advanced microelectronics packaging requires inspection workflows that preserve multiscale context while enabling rapid, repeatable access to buried structures for microscopy and metrology. Preparation methods often impose a throughput–fidelity tradeoff: fully serial high-precision approaches (e.g., FIB) scale poorly for large access, while faster bulk removal can introduce redeposition, roughness, and boundary artifacts that reduce SEM interpretability. We present a correlative characterization framework that couples navigation, ultrafast-laser access, and targeted FIB/SEM refinement to enable inspection-grade access across heterogeneous package stacks.

The workflow follows a "map → access → verify → refine" loop. When available, X-ray CT provides 3D localization and access constraints in intact assemblies. Ultrafast-laser processing then produces microscopy-oriented access modes—decapsulation/delayering-style exposure, millimeter-scale cross-sections, and localized access windows—parameterized to prioritize edge integrity, low redeposition, controllable taper, and stable geometry. Optical microscopy and confocal topography verify placement and depth progression, while SEM resolves interfaces and defect-relevant features. Brief localized FIB steps are applied only when nanoscale finishing is required, shifting FIB from bulk removal to final refinement.

Representative results show that in-process artifact suppression supports aggressive removal while maintaining a narrow collateral-affected region at cross-section boundaries (below ~150 nm in representative measurements, including operation up to ~24 J/cm²). For localized access windows, symmetry-preserving scan paths and real-time debris management improve circularity, reduce redeposition, and stabilize taper, enabling consistent apertures for repeated metrology sites. Overall, this framework unifies device-to-package navigation and microscopy-ready access into a scalable pipeline that reduces preparation latency while preserving measurement confidence for metrology, inspection, and failure analysis in advanced packaging.

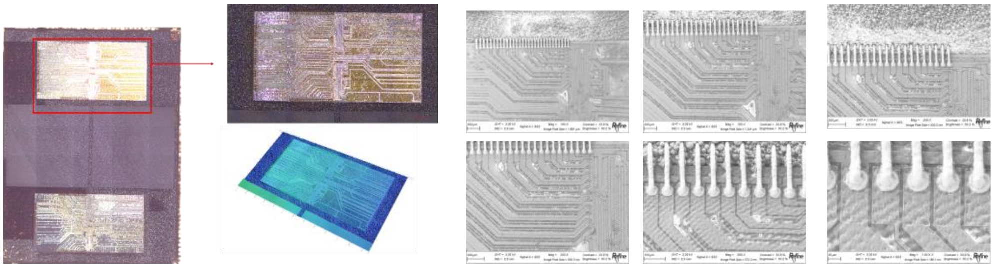

Figure 1: A15 package after laser-only decapsulation (removal of the epoxy encapsulant) using Tescan FemtoChisel. Previously buried surface features are revealed, including circuitry associated with two DRAM regions and two silicon structural blocks. Corresponding optical, confocal, and SEM images are shown.

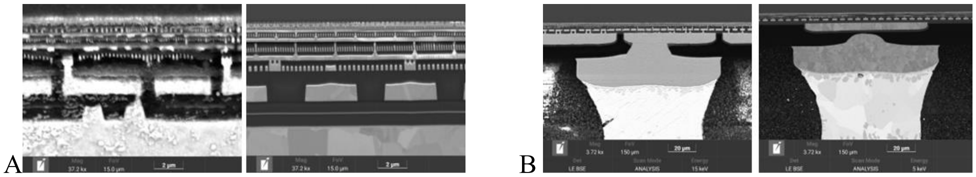

Figure 2: Two instances of gas-assisted, LPL (laser protective layer)-enabled femtosecond-laser cross-sectioning of advanced microelectronics packages (A and B) using Tescan FemtoChisel. In each section left shows before and right shows after polishing with FIB.

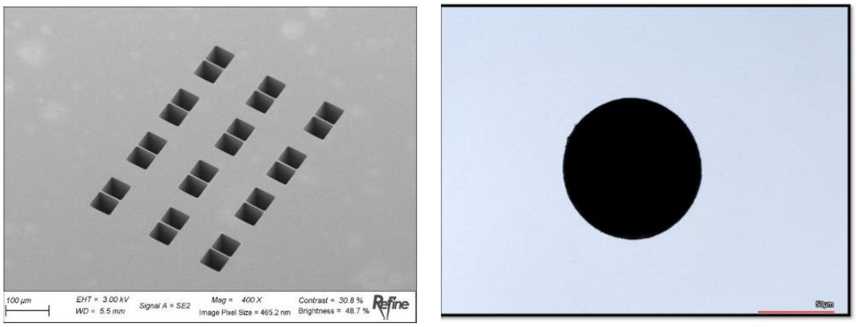

Figure 3: Left: Laser-enabled batch pre-lamella preparation in silicon using Tescan FemtoChisel; Laser-enabled hole formation in silicon using Tescan FemtoChisel.