Self-Aligned Nanoscale Trench Etch In Silicon Using Mask Thickening With Convex Corner Lithography

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This work demonstrates a new fabrication process, essential for the fabrication of parallel arrays of three dimensional (3D) nanodevices. It combines self-aligned so-called convex corner lithography (CxCL) with nanoscale cryogenic plasma etching. An important problem that was solved is the required thickening of the nanoscale mask, related to the thinner thermal silicon dioxide (t-SiO_2) mask near the apices and the limited etch selectivity. Applications are manifold, including nanophotonics, nanoelectronics, and nanoelectromechanical systems[1] where this fabrication process can be an important step in novel 3D fabrication schemes.

This process starts with wedges in silicon (Si) made with anisotropic wet etching of Si. By using low temperature dry thermal oxidation and isotropic etching, self-aligned ~10 nm openings in the t-SiO_2 CxCL are fabricated (Figure 1A)[2]. The t-SiO_2 mask thickness ($t_{mask,1}$) is thin near the nanogaps, which, combined with low cryogenic etching selectivity, requires mask thickening for obtaining deeper trenches. Therefore, initial trenches are first etched (Figure 1B) which define the final t-SiO_2 mask thickness ($t_{mask,2}$). The trenches are refilled with LPCVD silicon nitride (Si_3N_4), and selectively etched back using wet isotropic etching[3] (Figure 1C). Combining this with thermal oxidation of Si, results in an increasing t-SiO_2 mask thickness along the trench depth while the trenches are protected (Figure 1D). By selective wet etching of Si_3N_4, the trenches are emptied, and the Si is reached as shown in Figure 1E. This provides the opportunity to continue trench etching.

Figures 2I and 2II present cross-sectional SEM images using $t_{mask,1}$ and $t_{mask,2}$ respectively, both prior to (') and following (") 60 seconds of plasma etching under identical conditions. The top width increases from 10 nm to 126 nm for $t_{mask,1}$, but only from 33 nm to 44 nm for $t_{mask,2}$. Additionally, the trench depth nearly doubles in the thickened mask sample: 232 nm for $t_{mask,1}$ vs. 406 nm for $t_{mask,2}$. These results demonstrate that the mask thickening procedure significantly improves the etch performance for nanoscale trench etching applications.

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[1] Laermer, F., Franssila, S., Sainiemi, L. & Kolari, K. Deep reactive ion etching. in *Handbook of Silicon Based MEMS Materials and Technologies* 417–446 (Elsevier, 2020). doi:10.1016/B978-0-12-817786-0.00016-5.

[2] Berenschot, E. *et al.* Self-Aligned Crystallographic Multiplication of Nanoscale Silicon Wedges for High-Density Fabrication of 3D Nanodevices. *ACS Appl Nano Mater* 5, 15847–15854 (2022).

[3] H. Mertens *et al.*, "Forksheet FETs for advanced CMOS scaling: Forksheet–nanosheet co-integration and dual work-function metal gates at 17 nm N–P space," in *2021 Symposium on VLSI Technology*, Kyoto, Japan, pp. 1–2 (2021).

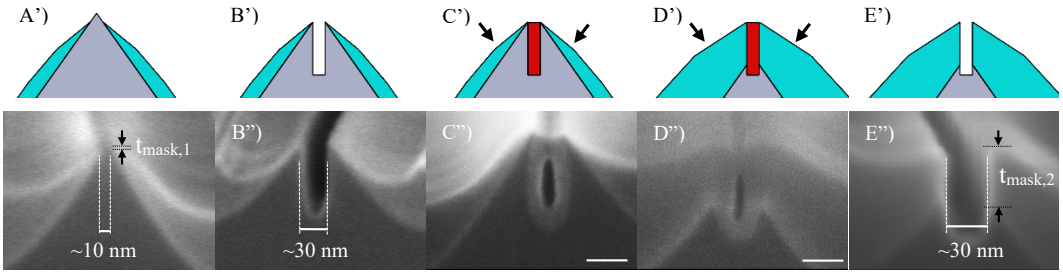

Figure 1: cross-sectional schematic (') and SEM images (") of the proposed fabrication process. A) isotropic wet etching t-SiO_2 resulting in ~10 nm mask opening with mask thickness $t_{mask,1}$, B) cryogenic plasma etching of Si widening the top width to ~30 nm, C) refilled trench with Si_3N_4 after back etching, D) dry thermal oxidation using Si_3N_4 as hard mask, E) selective etching of Si_3N_4 showing mask thickness $t_{mask,2}$. Scalebars are 30 nm.

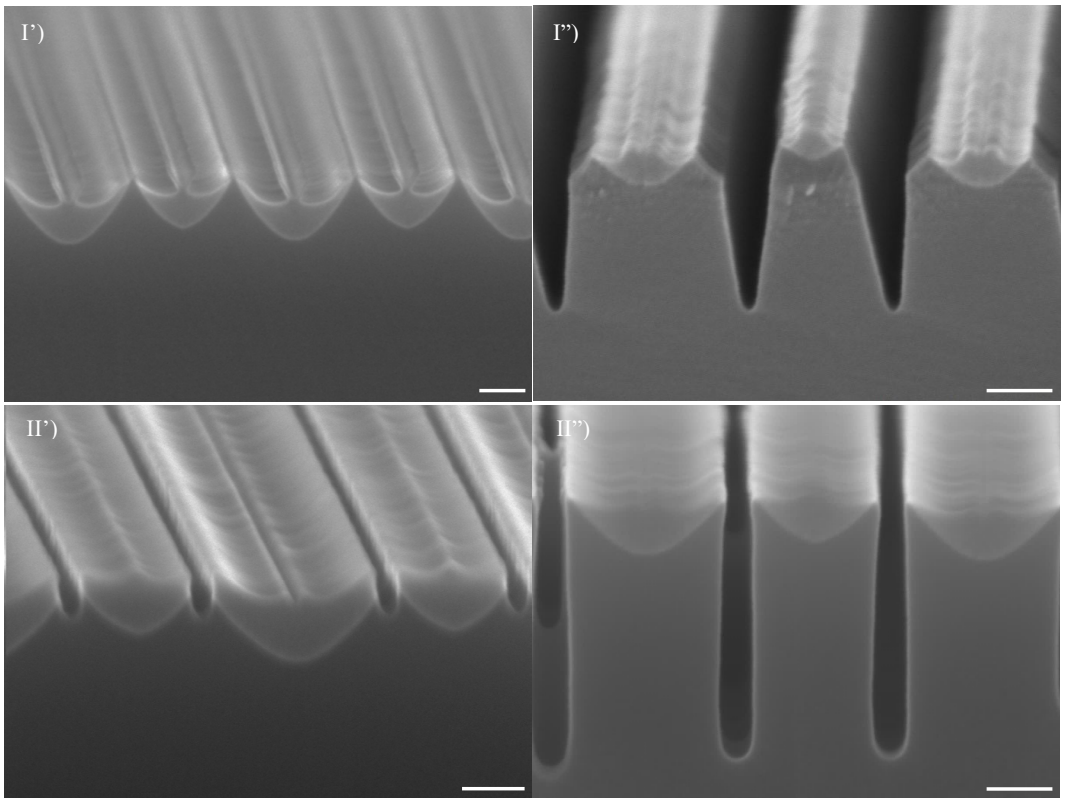

Figure 2: cross-sectional SEM images without (I) and with (II) the mask thickening procedure before (') and after (") 60 seconds plasma etching under identical conditions. Scalebars are 100 nm.