In-device overlay study using high landing-energy SEM and VC during backside patterning in CFET technology

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In view of the continuous scaling of the semiconductor devices, development of complementary FET (CFET)[1,2] and BSPDN technology is of great importance. In the CFET architecture, to comply with the scaling limitations, n-type and p-type transistors are stacked on top of each other, requiring wafer-2-wafer (W2W) bonding and multiple backside layer EUV patterning. The W2W bonding yields distortion on the wafer and thus creates critical overlay challenges during backside metal and via patterning. Therefore, it is important to measure overlay at the device feature to be able to gather information more precisely and locally, compared to the measurement at the metrology box. Moreover, the uniformity and quality of via placement on the metal line is essential to have lower resistance and higher yield. Non-availability of the traditional overlay marker at the device feature emphasizes the necessity of in-device metrology. This work can be an alternative to the traditional overlay measurement at the metrology box and at the same time can provide useful information on local deformation introduced during W2W bonding.

We are exploring a key backside via-to-metal (BSV0D-to-BSM0, Figure 1) connection using high landing energy SEM images and voltage contrast (VC) signal. We are investigating the effect of programmed overlay on in-device metrology and inspection. Based on the design, we will introduce different expansion factors on the wafers to produce different overlay offsets in ±X direction. To collect the SEM images at the device feature, we will be using high landing energy so that there is enough beam penetration to obtain well-resolved via and metal images (Figure 1). In this way we can obtain localized overlay information and account for the local and non-linear distortion induced by W2W bonding. In addition to high landing energy SEM imaging, we will also implement VC imaging to obtain insights into the quality of via connection to the metal. This will demonstrate differences in charging behavior across the wafer in ±X direction. The correlation between VC gray-level values and overlay in ±X (Figure 2) can be used to demonstrate how via is placed on the metal (contact uniformity or non-uniformity) and has the capability to be utilized as fast and non-destructive way to estimate in-device overlay performance of the backside layers. Altogether, this work has the potential to move a significant step forward towards in-device metrology to be applied for backside layers in W2W bonding.

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[1] P. Schuddinck et al., in 2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits) (2022), pp. 365–366.

[2] S. Demuynck et al., in 2024 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits) (2024), pp. 1–2.

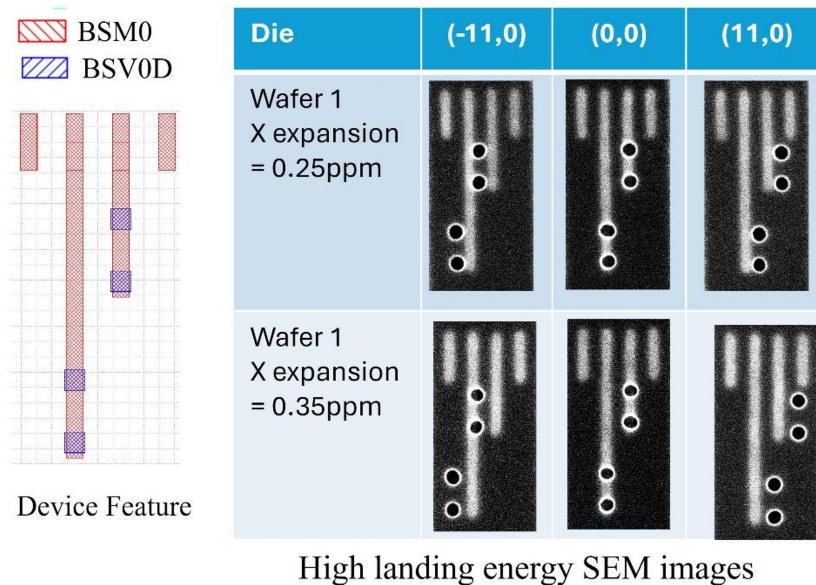

Figure 1. Design of the device feature of backside metal and via layers (BSM0 and BSV0D, respectively), and the corresponding high landing energy SEM images obtained on programmed overlay wafers at the left edge (Die -11,0), mid area (Die 0,0), and right side (Die 11,0) of the wafers.

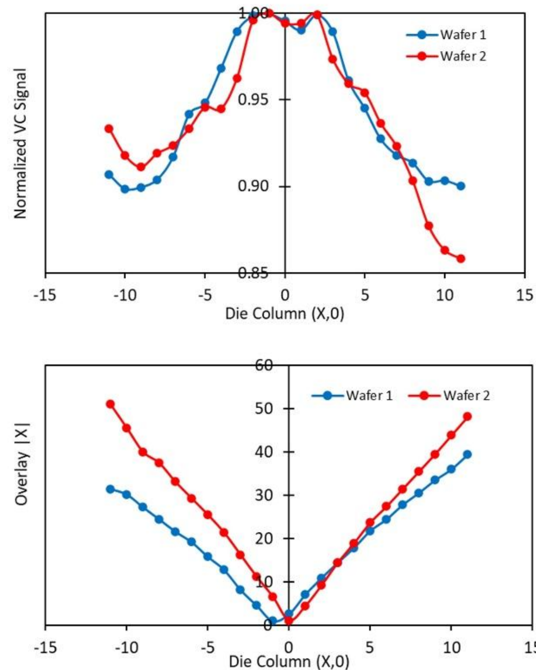

Figure 2. Correlation of the voltage contrast (VC) signal with the overlay values in ±X direction across the wafers.