Fabrication of nanostructured silicon standards for Atom Probe Tomography

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Atom Probe Tomography (APT) is a powerful analytical tool that combines field ionization of atom and time-of-flight mass spectrometry techniques to create a spatio-elemental 3D- map of atoms with sub-nanometer accuracy and parts-per-million sensitivity. [1] This combination of capabilities makes APT an ideal technique for semiconductor applications in R&D, failure analysis, etc. [2] However, the current reality is that the technique often falls short of its potential due to a number of different variables related to sample prep, experimental conditions, and data analysis techniques. These limitations have slowed adoption of the technique in near-line metrology workflows in some parts of the industry and often limits its application to simple and well-behaved structures and materials. One possible solution to overcoming these limitations is using standardized practices and reference materials for benchmarking measurement accuracy and uncertainty, as well as tool-to-tool performance. The work to be presented here will describe the development of potential reference materials for assessing the fidelity of 3-D APT reconstructions using simple-to-fabricate structures with known geometry and relevant materials for modern FEOL device structures.

To create these structures, we used a combination of standard fabrication techniques, including e-beam lithography, dry and wet etching, and ALD/PECVD. The fact that wet etching of Si <100> in potassium hydroxide solution preferentially attacks the 100 planes resulting in characteristic anisotropic V-shaped trenches with sidewall angles of 54.74 ° from the surface [3], was exploited in this work to create features with a consistent and predictable geometry. Nanostructured arrays of line gratings and isolated square features were transferred through a SiN_x hard mask onto the silicon wafers. Several combinations of line width/pitch for gratings and square side/pitch for grids were incorporated in the layout design. The final anisotropic etching of silicon using KOH resulted in V-shaped trenches for the line grating and inverted pyramidal holes for the square grid patterns, respectively. The trenches and inverted pyramids were then conformally coated with HfO_2 (~10nm)/SiO_2(~ 40 nm) using an ALD tool followed by a coating of e-beam Si (~ 150 nm) for both materials contrast and plugging any possible gaps. APT specimens were prepared using standard FIB-based preparation such that a single feature was contained in the sample near the apex. A 3-D reconstruction of an APT data set and a corresponding STEM image for a V-trench (Fig. 1) shows as proof-of-principle that the proposed standards could be used as reliable industrial standards for APT.

References:

[1] T. F. Kelly and M. K. Miller, Review of Scientific Instruments 78, 031101 (2007).
[2] B. Gault *et al.*, Nature Reviews Methods Primers 1, 51 (2021).
[3] K. E. Bean, IEEE Trans Electron Devices 25, 1185 (1978).

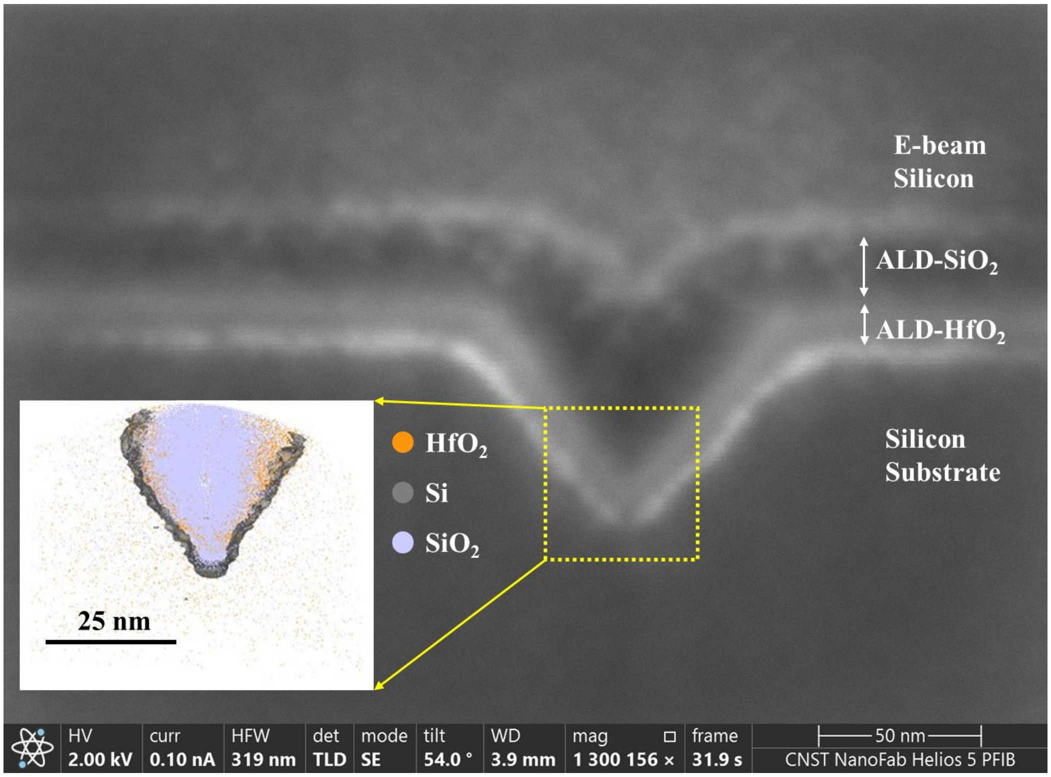

Fig. 1: SEM cross-sectional view of a V-shaped trench with the characteristic slope in <100> silicon fabricated via wet etching of a 30 nm linewidth pattern transferred through SiN_x mask using e-beam lithography. The inset shows a data reconstruction of the same structure using atomic probe tomography tool.