A Stochastic Analog SAT Solver for Intrinsic Stitch Optimization in Multiple Patterning Lithography Layout Decomposition

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Multiple patterning lithography is essential for advanced nanofabrication as feature sizes continue to scale beyond the resolution limits of optical lithography. Triple (or more) Patterning Lithography (TPL) layout decomposition seeks to assign layout features to three (or more) masks without conflicts; however, dense layouts are often inherently non-three-colorable due to topological constraints in the conflict graph. Stitch insertion, which splits features across masks, is therefore required to improve decomposability, but excessive or redundant stitches increase layout complexity and degrade yield. Conventional software-based decomposition methods rely on computationally intensive graph analysis and iterative optimization, which limits their scalability for large, complex designs.[1]

In our previous work, we demonstrated the feasibility of using a stochastic analog 3-SAT solver[2] to accelerate the layout decomposition process with extraordinary efficiency.[3], Yet the approach only works for a fully decomposable layout. In this work, to account for the non-decomposable case, we present a modification to the SAT solver that enables intrinsic stitch optimization during layout decomposition. The decomposition problem is formulated as a graph coloring task and mapped to a 3-SAT representation. Stitch candidates are generated by locating discontinuities along violation edges, a process that can be completed in polynomial time. Conflict constraints are encoded as hard clauses, while stitch insertion is modeled using soft clauses, allowing the circuit to suppress redundant stitches while preserving those required for colorability. By exploiting analog dynamics and massive parallelism, the proposed solver rapidly converges to optimized solutions with minimal stitch count, demonstrating a promising hardware-based approach for efficient multiple-patterning layout decomposition in advanced nanofabrication.

Figure 1 shows the flow for layout decomposition with stitch optimization. The process begins with a software detection of spacing violations and the creation of a violation edge of a three non-colorable pattern. The Stitches candidate is then generated by identifying discontinuities in the violation edge, as depicted in *Figure 2*. The processed pattern is then transformed into a 3-SAT problem with hard and soft clauses, representing coloring conflicts and stitches, respectively. The problem is fed into the proposed circuit as shown in *Figure 3*. *Figure 4* presents the SPICE simulation results of the proposed circuit's solving process, along with the final decomposed layout. The circuit effectively eliminates redundant stitch candidates while preserving only the necessary stitches, thereby achieving an optimal coloring solution with minimal stitch insertion.

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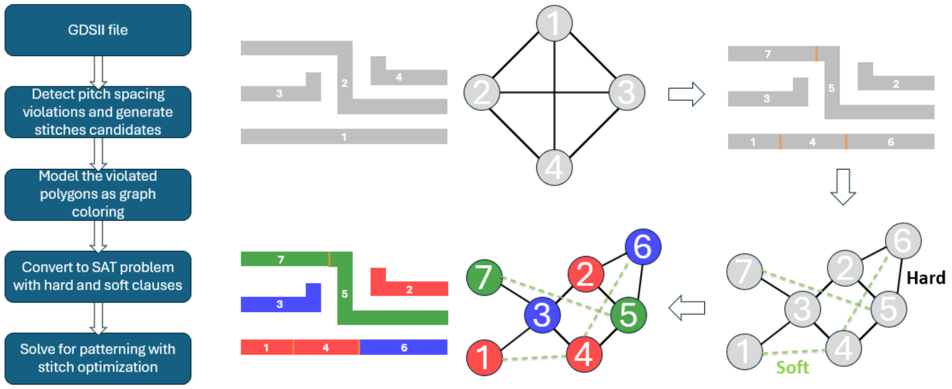

Figure 1: Layout decomposition flow with stitch generation and optimization.

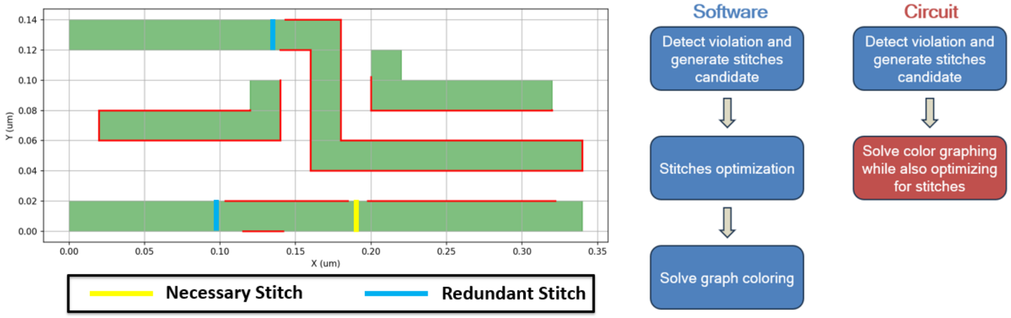

Figure 2: Example Stitch candidates generated by violation edge overlapping and comparison between the proposed circuit approach versus the Software approach for stitch optimization.

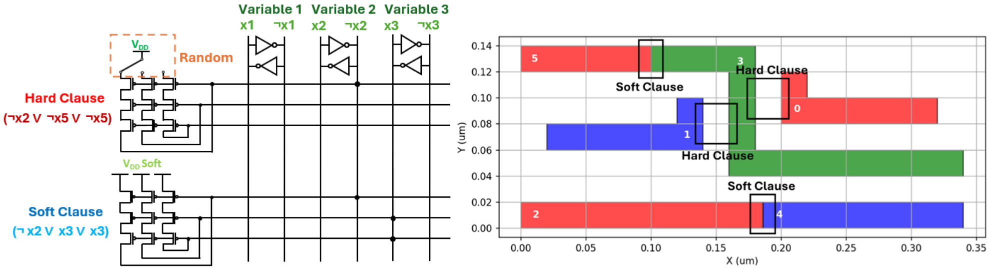

Figure 3: The modification of the circuit to enable intrinsic stitch optimization. Stitches candidates are modeled as soft clauses and implemented with a weaker V_{DD}.

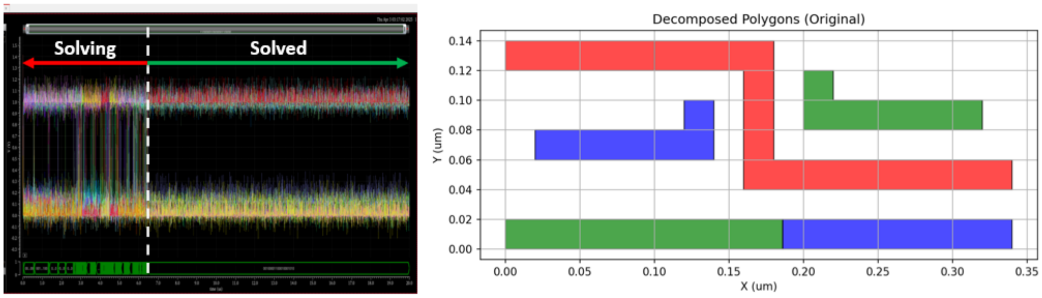

Figure 4: SPICE simulation of the circuit and the resulting decomposed pattern showing an optimized stitch insertion location.